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**PCB Designers:
The Next Generation**
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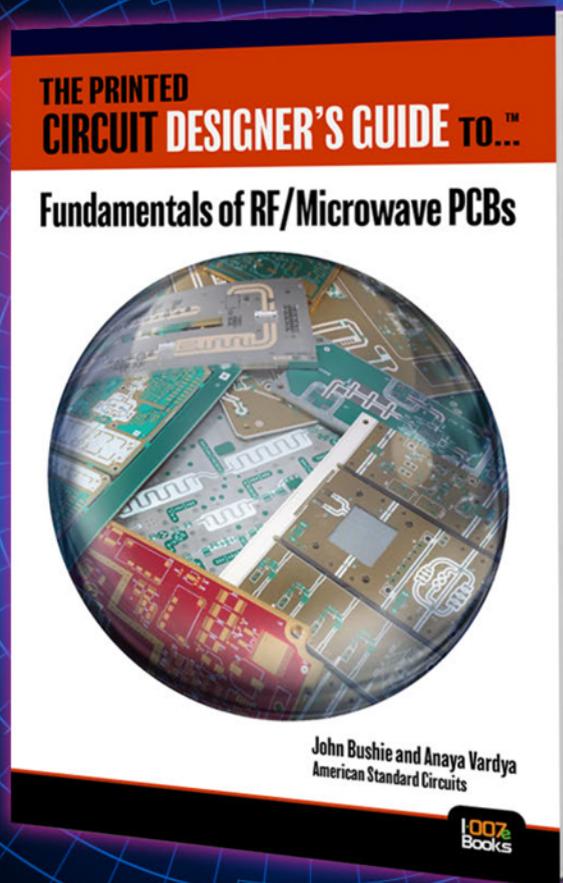
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PCB Designers: The Next Generation

For the past decade or so, we've watched as North America's PCB designers began reaching retirement age. The problem is that not many young people are entering the field of PCB design, and outgoing senior designers' positions are increasingly being covered by design engineers. This month, we ask, "Who are the next generation of PCB designers?"



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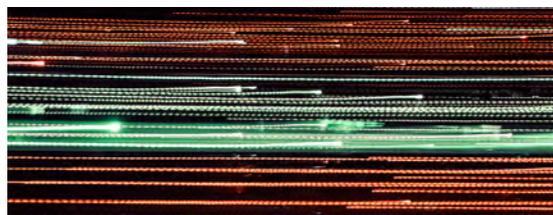
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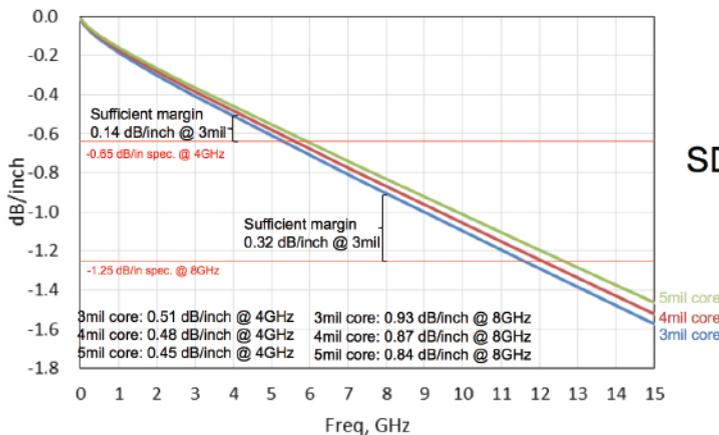
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Td-5%(°C)	TGA 5% loss	380
CTE (%), 50-260°C	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

IT-170GRA1 Insertion Loss



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Who Are the Next-Gen Designers?

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When was the last time you met a young PCB designer? I'll wait.

I meet two or three young designers each year, but then again, I'm actively looking for them, like Sherlock Holmes on the trail of an elusive suspect. And young designers are hot property. Find a young designer at a trade show or conference today and you'll usually find a crowd of designers peppering him (or her, in one recent case) with questions.

"Where do you work? What tools do you use? What courses are you taking here? Take this SI class. Introduce yourself to each speaker after class. Is there a Designers Council where you live?"

When young PCB designers at an industry trade show get celebrity treatment, that's a

worrying sign. But we've been watching these signs for years as our friends and colleagues "graybeard" out of the industry.

When I started covering this industry in the '90s, I was 36, a little younger than the average designer. Now I'm getting AARP mail, and I'm still younger than most designers, because the retirees are not being replaced at anything near a 1:1 rate.

Hundreds of smart young people discovered the PCB design career in the '60s, '70s and '80s, at a time when there was no Internet, and very few conferences and trade shows. Now we have dozens of ways to spread the word about PCB design—an interesting, critical, good-paying job—and all we see is a trickle of young designers coming into the field. And



most of the young designers I've met recently are engineers, electrical or otherwise. Is there a future for the "pureplay" non-degreed PCB designer?

As our featured contributors explain in this month's issue, you have to go directly to the young people, because they're not going to find us. Some companies have set up programs with nearby universities, and others visit high schools or get involved with Maker Faire events, or sponsor a team of students for a robot competition. We all need to be missionaries, doing whatever we can do to spread the gospel of PCB design to the unconverted.

It helps to think big. This year's IPC APEX EXPO introduced quite a few young people to the PCB community. IPC's Design Program Manager Nancy Jaster invited students from two San Diego high schools to attend the expo as part of the organization's new STEM Outreach program. The students were everywhere, talking to attendees and exhibitors and staring wide-eyed at the machines on display. You can bet that most of these kids had no idea that this industry even existed before this visit.

Also during IPC APEX EXPO, we invited photography majors to participate in our [I-Connect007 Student Photo Contest](#). The students shot 750 photos during the show, many of them professional quality shots. They fleshed out their portfolios and learned a lot about circuit boards.

This is what it takes. We have to go to where the young people are and tell them all about this industry that we love, because they're not going to find us on their own.

Our first feature is an interview with Fairfield Geotechnologies' Susy Webb, who has been teaching her class "The Basics of PCB Design" at PCB West for years. Over time, Susy's attendees have switched from a room-

ful of designers to almost entirely engineers, so we asked for her thoughts and a few stories about educating the next generation of PCB designers.

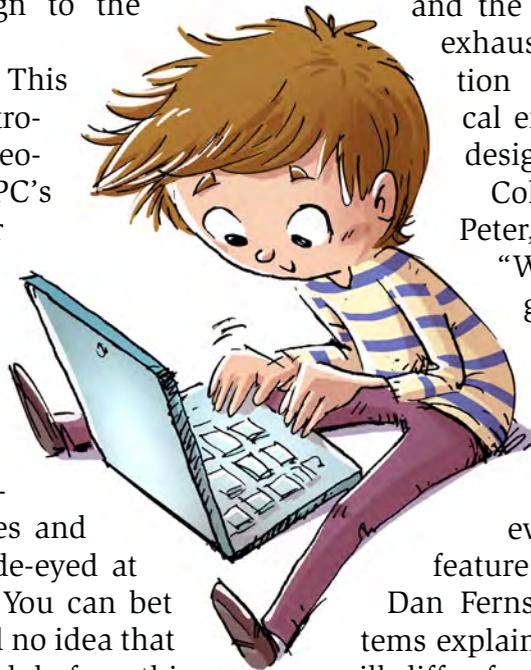
Next is an article by Mike Creeden, CID + , of San Diego PCB. Mike discusses the "changing of the guard," some misconceptions that managers have regarding the art of PCB layout, and why asking electrical engineers to design today's high-speed PCBs may be easier said than done. Our third feature is an interview with Mentor's Paul Musto, who explained the company's relationship with universities, and the need for designers to have an exhaustive knowledge of the fabrication process, which many electrical engineers may lack as they start designing boards.

Columnist Tim Haag channels Peter, Paul and Mary by asking, "Where have all the designers gone?" He discusses the need for the "old guard" of PCB designers to pass on their knowledge to the youngsters, and some of the ways the job requirements for a designer have evolved over the years. And in a feature interview, Bryan LaPointe and Dan Fernsebner of Cadence Design Systems explain how designers of Generation Z will differ from their predecessors, and what can be done to bring more smart, young people into the design community.

We also have columns from regular contributors Barry Olney and Phil Kinner, as well as a great technical article from Yuriy Shlepnev, president of Simberian Inc.

No one knows exactly what the next-gen PCB designer will look like, but change is coming. And isn't change one of the best things about your job? Never a dull moment!

See you next month. **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking [here](#).



Susy Webb: Training the New Generation of Designers

Feature by Andy Shaughnessy
I-CONNECT007

For years, I've been running into Susy Webb at PCB West, where one of the classes she teaches is PCB design basics. I always ask Susy about the class, especially the attendees' backgrounds. Over the years, her class has begun drawing more and more degreed engineers, with fewer "traditional" PCB designers attending.

In this conference call with I-Connect007 Editors Happy Holden and Patty Goldman, I asked Susy to discuss the next generation of PCB designers, some of the trends she's seeing among new PCB designers, and the need for designers to take charge of their own design training, whether their management agrees or not.

Andy Shaughnessy: Susy, you teach a PCB basics class. Why don't you give us a quick review of the class and what you teach in the class?

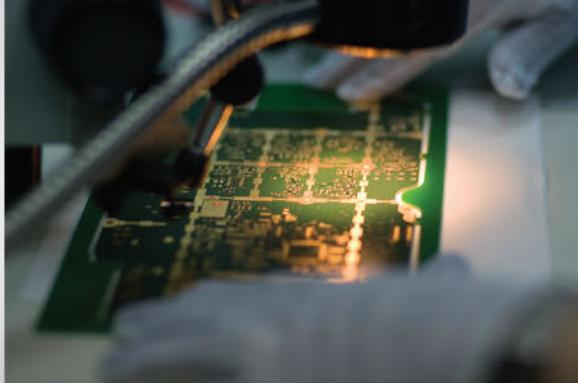
Susy Webb: The class started out as a two-day class and it has changed over the years, sometimes going down to half a day and sometimes up to a full day. For the last few years it's been a full day class. There's way more material than can be covered in one day, so that requires me to step back to 10,000 feet and shoot at the major topics involved with design like building library parts, placement, and routing techniques. Since it's a basics class, I never know ahead of time whether I'll be getting somebody who's been pulled into the realm of design from other areas, and is completely new to design.

Some people come in that way, needing the absolute basics, or some people come in for a refresher, or as engineers, and they all want slightly different information discussed in the class, and when there is just one day, you do what you can do. I do explain that when we start the class. So it can be rather basic for some and sometimes over-the-head for others. It's a hard line to draw to figure out what goes into a class and what doesn't.

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Shaughnessy: I started asking you about your class years ago, and it was almost all designers with the occasional engineer. Tell us how that's changed.

Webb: I do think it's been gradual. My honest opinion is that most engineers don't really want to design boards, they just want the designs done right, and the boards to function properly.



Susy Webb

The technology has changed so much and the vision that engineers and their management still have is of designers being connect-the-dots kind of people. So, that leaves it to engineers to pick up the gauntlet and move forward with it. And that's not a bash on engineers at all; I'm glad they want to know about

PCB design. But I don't think they want to be a designer full time. I think they want to be engineers, designing and testing circuits rather than designing boards. Both have equal challenges and both have equal rewards. But if you've been trained in college to be a circuit designer, you don't necessarily want to design the board as well.

Designing has gotten so much more complex over last 15–20 years, and perceptions have not kept up. People tend to think that the engineers need to do it, but that's not necessarily the case. I believe that the people who have been in the field, or are interested in the field, need to work at getting training and continuously learning in order to show managers that they have what it takes. They also need to push their management to pay for the training they need, so that they can deliver the best product. Because it's challenging. You have to understand how the signals work within the board structure itself, as opposed to understanding how this signal needs to connect to that part, and everything else that goes with it.

Shaughnessy: Do you find that the EEs in your class get any sort of PCB layout experience in college, any sort of education on PCB design?

Webb: You're going to pin me against the wall on that issue [laughs]. I understand that many engineers have been taught to design a simple circuit and make it into a simple board, and maybe even have it fabricated and assembled. So they say, "Yeah, I've done a board." But that's not really what board design is all about.

So they may have some experience, but it might not be by any stretch of the imagination what will be required on the typical high-speed, controlled impedance board with complex stack-up control, and all the things that requires. None of them are taught how to design for fabrication or assembly, or what might work best for testing. Nor are they taught how the signals might interact with each other, how the return current will work, or what constitutes a good fabrication package to send to fab and assembly. Unfortunately I don't think they're taught any of that in college.

Shaughnessy: And this last year at PCB West you had 20 attendees, and they were pretty much all engineers, isn't that right?

Webb: Yes. It's certainly more engineers, with the occasional newcomer to the field too. But they're more often engineers, and I'm glad to see them. If they are going to design the boards, they need to learn the right way to do it. Because nothing we do as designers is done randomly; it's done because of the domino effect that might be created down the road. What we do affects the assembly, fabrication, the electronics involved, and more. If you put the parts in the wrong position, you're affecting how well the electronics will work, so you MUST understand what you're doing, how the parts will work together or the negative impact they might have on each other. Connecting the dots has not been the correct way to design boards, for many years.

I see all this as a need for whoever is going to be designing the boards—a newcomer, a person who has been in the field for a while, or

an engineer—to get some quality training, and that doesn't mean EE training. It means training at conferences and classes that are offered around the country for signal integrity, EMI, DFM, HDI, etc., so that they understand what they should do, and why.

Shaughnessy: Is this generally people who are sent by their company, or are these people who just decided on their own that they need to go to this class?

Webb: Personally, I always did it on my own, but I think I'm not typical in that respect. I think people will ask their companies and their companies will say, "No, we can't send designers, but we'll send the engineers." And that's unfortunate. I will use the term "rules" loosely here, but there are rules that need to be followed. I use it loosely because of course we have to break the rules a lot of times. The engineering rules may break the assembly rules and the assembly rules may break the fabrication rules, so we have to know what the rules are all about (and their priority on any particular board) to know how and when to break them. Again, not a random thing. As I said, I use the term rules loosely because it's not set in stone that you have to ALWAYS do things a certain way.

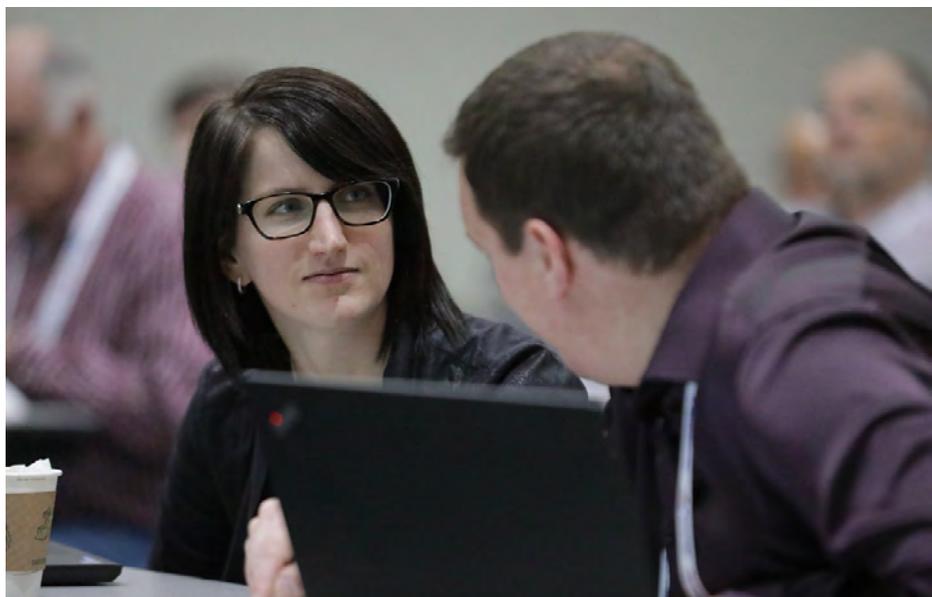
Shaughnessy: I bet the engineers probably ask different questions during the class.

Webb: They do. Engineers will ask more technical questions which is great. Unfortunately, some people don't realize what they don't know, so they don't know what questions to ask. I do my best to present what and why of the most important issues, and of course allow as much time as possible for any questions. On the evaluations, sometimes participants will say that it's not technical enough. But the evaluations of the people who are just coming into the business will say it's way over their head.

Each class attendee needs to come away feeling like they understood the material. If not, I hope they will ask for clarification in class or email me later. I always give them my email address. I want people to understand so that they are able to go back and do good work! This could easily be a week-long class if somebody wanted to sponsor it, and I have done it that way. There is just so much information to discuss. As the senior designers start to retire, there's going to be less mentoring available for the newer people who design boards. Who's going to teach them?

Shaughnessy: Right. Some senior designers started their careers by shadowing another designer for six months. But in most companies, there's no mentoring.

Webb: It's very different now. And there needs to be more of an emphasis placed on that while there are still designers around to help the newer people. So going to classes and glean some knowledge from the class, even if you don't understand at all, is a way to say, "I heard such and such; am I supposed to do that here, or is this more important?" As I mentioned, the EEs are very good at what they do, but following the signal around from layer to layer of the board is not necessarily anything they were ever taught and the environment on different layers of the board can be very different.



Shaughnessy: That's true. We hear about the "brain drain," where a lot of designers retired or left the industry during the 2002 and 2008 downturns.

Webb: Yes, I see it as not a "brain drain" but as "expertise drain." But yes, we did lose a lot of people at that point. I also read an article about designers retiring, and within the next five years we could lose 25–50% of designers. Something has to be done so that we don't lose all that knowledge.

Shaughnessy: It's a real issue. But I am seeing more young people. Are these primarily young people in your class?

Webb: There are certainly a few people who have been around a while, probably engineers who have never been asked to do that kind of thing, and there are a few of the older people who got out of the business in 2008 or whatever and are trying to get a refresher to get back in. And there are some younger people too. It's a mix. The problem for younger people is that they don't really know about PCB design as a career while they are in school, so they may not know to pursue that area without a gentle push.

Shaughnessy: Could an influx of EEs doing design be a good thing? We keep seeing all the signal integrity and EMC problems that designers have now. Will designers of the future need to have some engineering background?

Webb: Oh, yeah! Every bit of knowledge improves the whole and designers and engineers working together would be a very good

thing. Designers didn't need to know what high-speed design was when I first started in this field, much less how it was defined and how to adjust for it. We didn't understand electromagnetic fields and return current and why they would become important in the future. But as technology has changed, so has the need for knowledge. So, yes, I definitely think that whoever's going to design the board needs to have a lot of technical information about how the electronics will work inside the board itself. And neither group has been taught

that unless they have pushed themselves. I have bought lots of engineering books and attended a lot of classes and slogged my way through them trying to understand what they're saying because I didn't have an engineering background, and so I have learned and trained myself in that way.

I think the designers have to be their own advocates and find a way to get the training they need. Things are constantly moving forward and changing constantly. I

remember when I went to my very first class ever taught by Rick Hartley in Austin. I didn't understand half of what he said, but I stuck with it and I've gone to several more of his over the years.

The point is that Rick was also designing at much lower speeds back in the early '90s and yet what he taught was new to me. As today's speeds get faster and faster, all of us have to adjust and figure out what the changes need to be with the way we do things. If we don't continue to learn, we won't be keeping up with what is current.

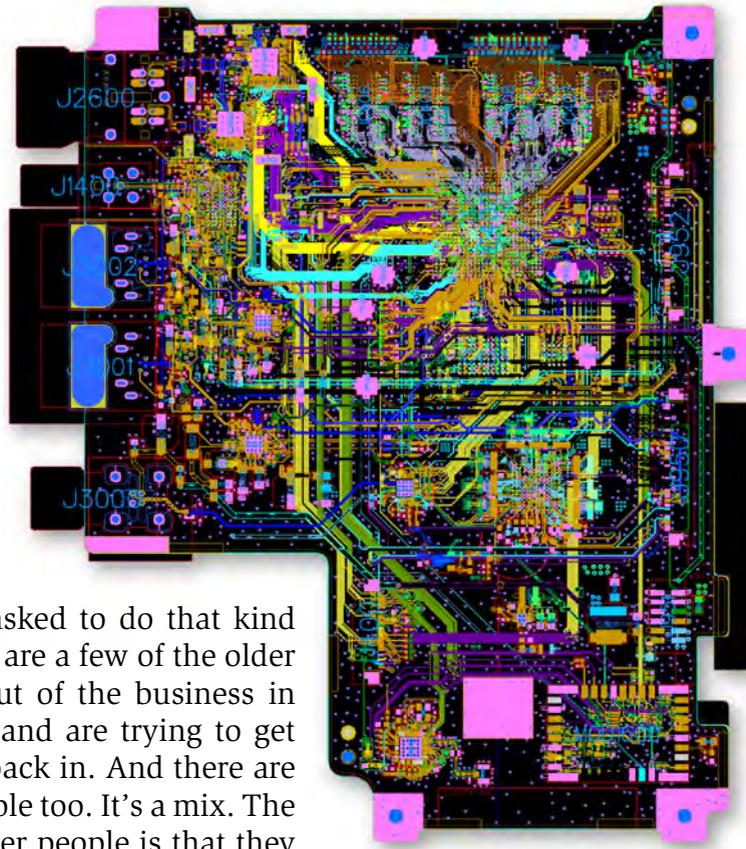


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Webb: I feel like the other countries are seeking information as well, probably on about the same level that the people here are. I've been to several different countries to teach, and I'm going to Australia in the fall for the third time. So I know that they are hungry to learn down there. I know the people in Europe are working hard to get good information, and they are talking to IPC about

Shaughnessy: If you put on your wizard hat, who are the designers of tomorrow?

Webb: I think there's an opportunity for people who don't have an engineering degree to continue in the business if they are a proponent of their own career, but if not, it will probably have to be more engineers, just because that part of business is more complicated as well. Sometimes I'm concerned there will be a dip in board expertise when designers leave the field through retirement, and engineers pick it up, because if they're not using the expertise that's available now for all the various facets of design, then they will have to learn the hard way.

Plus, when I got into really studying all of this and reading the books and whatnot, I thought it was black and white. But it's not really that way. There are differences of opinion even among the experts in the field. So designers and engineers have to keep up with the business, and ask questions of the people that have done their research and that they can trust.

Patty Goldman: There is concern about so many designers retiring in the next five years. Are other countries having the same problem? How about in the East? Are they churning out designers?

designers council chapters as well. If they get together and talk over a subject, they're learning. And so I would think that it's approximately the same in other countries.

Goldman: I guess my concern wouldn't be so much Europe as it would be Asia.

Webb: I know that there is a lot of reaching out from people in Asia and India to people in the U.S. asking questions and advice. They may not have the same access to conferences and to mentoring that people do here. So I think sometimes they get on LinkedIn or other design groups and ask questions there because that's the only method they have. At least they have the desire to know more, to understand more, to do their job correctly.

Goldman: I guess my concern is that pretty soon, not much is going to get designed in this country and that we're then dependent on other countries for things we need.

Webb: I hope that's not the case. It's impossible to know for sure, but I believe the best expertise is still currently in this country. But others are striving to produce quality boards too. I have been a judge for a contest, and many of the designs were from overseas. Many of them were really good designs.

Happy Holden: That's what I worry about it. There are a lot of foreign companies centered in the U.S. that are focused on outsourcing engineering, and they come in and talk to the bosses and say, "We'll do the PCB layout faster and cheaper so you don't need to educate or hire designers." And because of their large availability of engineers and people, they can take on the job. A lot of the time they don't have the technical skills, but the bosses don't know that until it's too late.

Webb: That's exactly how I feel, Happy. At my company we have occasionally outsourced some work, and each time we have had to make some major changes before it was actually produced. That's disappointing.

Holden: If we lose design, we lose the high ground, because design is the physical realization of the schematic and the bill of materials. They do everything on computer and paper about the schematic, but they don't know if it really works until it goes down onto a board and gets assembled. And we could lose the whole ball game.



Webb: I agree. I would love to find a soapbox and say, "Look, you guys, you need to pay attention to this or it's going to go away."

Holden: I have a question about some of these new students, these electrical engineers. Are any of them involved in occasional designing, where they'd been working on the project and now they've been told to lay out the PC board, but after they finish up this PC board they get to go onto the next project? So they may see this as just another task, but not as a profession?

Webb: Exactly my point when I said I don't think they want to be there. They're willing to do it to understand it and how it works in the board a little bit, but they're not really saying, "Oh, I really like this career, I want to do this career instead of the one I studied for in college."

Holden: That's a big problem if those people aren't kind of committed to learning everything about printed circuit design and the nuances, but just see it as an occasional side job to get through as fast as possible.

Webb: If you're an engineer and you look at it that way, you're not going to be thorough about the way you consider how the domino effect is going to affect all the other people that work with that board you just designed, nor are you going to remember all the things that have to be considered. It's easy to miss things. So yes, I agree that's a huge problem. It's a profession where you have to know a whole lot about a whole lot of things.

Holden: When you finish up teaching your class, do you provide a list of resources? How do they continue to learn?

Webb: I have not addressed that issue as completely as I might. I usually provide a list of speakers and books I use for reference, but that's not really enough. I do encourage them to attend as many PCB design events as they can. When I teach that basics class at PCB West, sometimes I will have people from that class who will follow me to all my other classes that week, and I think they see further references there. But more importantly, sometimes people come in for just that one day and go

away. That's unfortunate; maybe their company wouldn't let them stay away longer, or maybe they felt that class was all they needed.

There are all levels of training at the conferences. Going back to my first class with Rick in the early '90s when I only understood a little of the information, at least I understood part of it. I got some ideas about how things should be done better, rather than just doing what I had been doing for years before that. I hope everyone in the business will strive to continue learning.

Holden: Yes, because if they're coming to your class and they are relatively new, they're not going to know all of the nooks and crannies of design. So, what's their next step? Have you found any good books on printed circuit design? I haven't.

Webb: No, I haven't found anything that is comprehensive about designing. There are people out there who are looking at that possibility of coming up with comprehensive classes or books or courses. And as soon as someone gets that book or that class written, it will probably change because the technology is changing so quickly. The physics don't change, but the way we account for them sometimes does. A class you can always edit, and we all edit ours constantly, but books are a mammoth undertaking to edit and update.

I've changed every one of my classes, including the basics class. I change them constantly because I might think of a different way to say

something, or I find a new example to put in that might better show what I'm talking about. And I'm very much picture-oriented in my classes because I think that helps people to see what I'm talking about as opposed to just saying the words. I want them to see the words.

Shaughnessy: Is there anything we haven't mentioned that you'd like to talk about, Susy?

Webb: Just figure out a way to say, "People, get out there and learn something!" That would be great. But I think that goes both ways. Honestly, I've talked to many designers who've been given an opportunity, and they've said "No, I don't want to go to California, I don't want to take a day off work, or I'm too busy." Somebody has to address the designers and say, "You need to push this on management and make it happen." And I've pushed to the point of annoyance, I can tell you!

Holden: I find it interesting that the CAD companies teach how to use their tools, but not how to design a PC board. And designing a PC board is more than learning how to use a tool.

Webb: Exactly. And the managers who buy the products need to understand that.

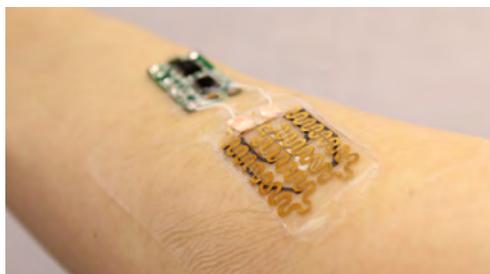
Shaughnessy: Well this has been really interesting, Susy. Thanks so much for your time.

Webb: Thank you, Andy. **DESIGN007**

Smart Bandages Designed to Monitor, Tailor, Treat Chronic Wounds

A team of engineers led by Tufts University has developed a prototype bandage designed to actively monitor the condition of chronic wounds and deliver appropriate drug treatments to improve the chances of healing.

"We've been able to take a new approach to bandages because of the emergence of flexible electronics," said Sameer Sonkusale, Ph.D. profes-



sor of electrical and computer engineering at Tufts University's School of Engineering.

Sonkusale and his team developed flexible sensors for oxygenation. A microprocessor reads the data from the sensors and can release drug on demand. The

smart bandages have been created and tested successfully under in vitro conditions. [Click here for more.](#)



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HELP WANTED: PCB Design Layout Specialist

Feature by Michael R. Creeden CID+, MIT
SAN DIEGO PCB DESIGN

The Changing of the Guard

I have been in this industry enough years to have heard the following question asked many times over: “Has anyone seen the next generation of PCB designers?”

This is a rhetorical question that has yet to be rightly answered. The typical response is a collective silence, at least until someone whispers, “No, we have not seen them, because for the most part, they don’t exist.”

For the sake of clarity and to help understand the nuance of my article, understand that the term “designer” is often utilized by many professionals. The term could apply to electrical engineers (EEs) doing schematic capture only, or one who performs schematic capture and layout, or anyone performing PCB layout. I will use the term “designer” to indicate specifically a “PCB layout specialist.”

I was told recently that the designer, aka the PCB layout specialist, is a dying breed soon to be extinct.

I wish to reassure my fellow designers as you read this article that, in my opinion, you are in the catbird seat. You are in hot demand and you should have great opportunities for the remainder of your career. By the way, after reading this article, you may feel empowered to go ask for a raise. Please don’t tell your manager that I sent you!

However, what I would ask you to do is ask around in your department and determine



the last time your company hired a beginner designer. What year was that? When did your office last hire a new, young designer, like you were once, at the start of your own career? Typically, it’s not occurring, and few new layout specialists are entering the profession.

The industry tends to ignore the subject of next-generation designer replacements. Historically, most layout designers would attest that the overall electronics industry ignores and disregards their profession. The electronics industry, for the most part, does not understand the PCB design profession. As long as the industry keeps paying your salary and you keep performing the “CAD miracle,” all things will keep moving along. But many of you are greybeards who can see the light at the end of the tunnel for your career exit. Good for you; in my opinion you deserve it!

This lack of new recruits is a phenomenon that is not unique to the design layout field. This is also occurring in the electronics industry on a broader level. Designers are few in number; therefore, little awareness is afforded our plight. The academic world attracts young

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people into the hardware and software engineering ranks in robust numbers. Within the EE degree programs there exist no significant PCB layout training or coursework. The number of academic institutions offering pathways into this very specialized profession of layout design is almost zero.

The number of academic institutions offering pathways into this very specialized profession of layout design is almost zero.

There are a few isolated examples of success in academia. A few seminar classes are taught at trade shows. I have had the privilege to contribute and serve with EPTAC Training Center to provide the IPC CID/CID+ certification program. But this program has the goal of taking an existing layout designer and broadening his knowledge base concerning manufacturing and electrical performance. It does not have the goal of creating a new designer. I have witnessed many people suggest that a simple MOOC-type class can be the solution to address the training need. Any designers worth their salt are laughing at this ridiculous perception because they know the realities and requirements of this profession.

So, what are we seeing in response to the designer shortage? The industry is looking for the EE to perform the task of PCB layout because they are assuming the EE is higher up on the food chain (no offense intended), and therefore they can just assume the responsibility of layout. Managers may provide EEs with EDA software design tool training. That is like assuming that knowing how to use a socket set makes me a qualified mechanic. This is also ridiculous logic!

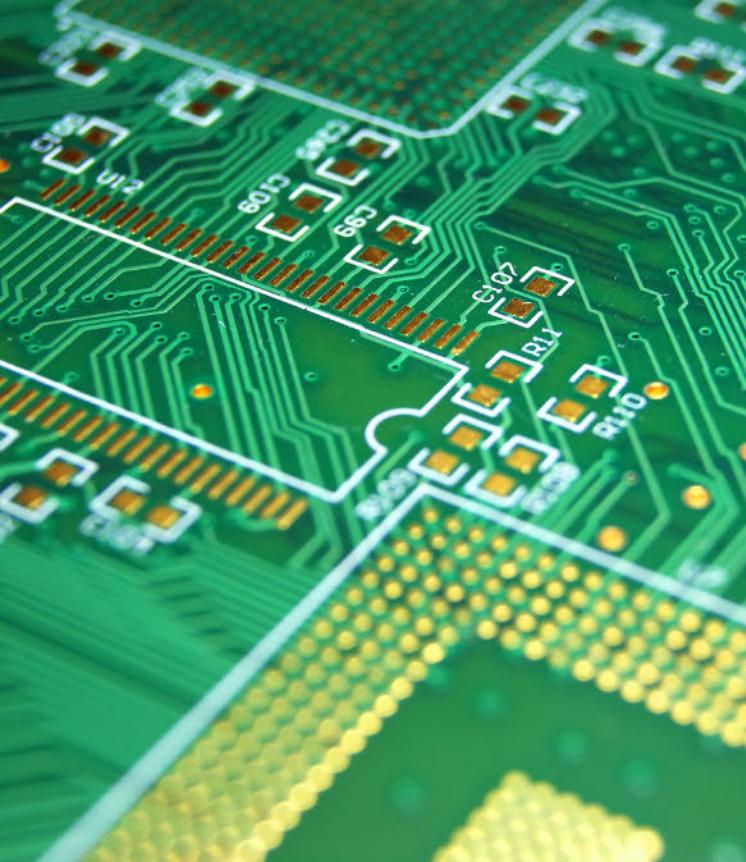
PCB design instructor Rick Hartley, who provides advanced signal integrity training, typically asks his students the following questions. To those who perform both schematic capture

and PCB layout, he asks, “Which of these two capacities is more difficult to perform?” Most of the time the answer is, “Layout is more difficult.” Then a follow-up question is asked, “How did you learn to perform the layout portion?” Typically, the answer is, “The school of hard knocks.”

Another point of note is that your average designer will perform layout after layout throughout the year, so they are continuously keeping sharp on their EDA tool and layout competency. They will be performing this for about 5-10 hardware engineers throughout the year. Do you think any one engineer once asked to do layouts will be performing layout for fellow engineers as a service or just themselves? The engineer now being asked to do layout, who is untrained in layout, will perform this portion of the development cycle about 3-5 times per year. At that rate of occurrence, the electrical engineers’ retention level is challenged, and proficiency will be difficult to maintain for both EDA tool usage and layout competency.

What else are we seeing as a response to the shortfall of qualified designers in the industry? The outsourcing model has been around for several decades now. Most domestic U.S. designers are negative on outsourcing from a job security concern, while most foreign designers are hopeful for the same reasons. Most businesses are keen to this idea at first, but later they often regret it. With the current distraction of today’s political climate of trade agreements and tariffs, we often love to accuse the other guy of creating this condition and the blame game is often fought by people blind to the truth—that it was businesses who wanted this and politicians on both sides delivered.

Businesses are way more capitalistic than they are democratic. Trade agreements enabled the access to reduced labor costs for reasons of corporate profits (research the history of NAFTA). Businesses are now having second thoughts about the concept of outsourcing, because it has led to a significant loss of intellectual property, substandard quality/producibility, and an increased frustration factor. Please keep in mind the words of Hartley



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who warned us about the short-sighted logic of, “Price is what you pay up front and cost is what you pay in the long run.”

What makes the role of the layout specialist so, well, special? Let me first explain a prevalent misconception that hurts our profession. Like the Mark Twain quote, the following expression puts the industry misconceptions into focus: “Some people are really smart; some people are really challenged, and some people open their mouths and remove all doubt.” I have heard some people in our industry say, “Layout is so easy that anyone can do it; after all, it’s just connecting the dots.” These are the decision-makers who don’t hire and train replacements, blindly outsource work overseas to save pennies and then request the EE perform layout without equipping them to be successful.

Back to my question of what makes the layout person a specialist. IPC Designers Council Executive Board created and submitted a working definition of the role of anyone performing PCB layout. This definition should be at the beginning of the IPC-222X Series Design Standard documents, available in its next release. The definition is helpful to understand the goals and qualifications to be successful.

Definition:

The professional role and responsibility to perform PCB design layout.

The following overview describes the core knowledge and competencies to best serve in this role of PCB design layout as a standalone professional or as the engineer performing this responsibility. Today’s designer must address three perspectives for success with the goal of making the first design iteration work as intended.

- **Layout Solvability:** Complex packaging skill set, including routing, placement, EDA tool proficiency, mechanical and thermal
- **Electrical Integrity:** Signal & power performance on all layers
- **Manufacturability:** DFX considerations of high yield and lower cost

The Result:

Maximum placement and routing density achieved, optimum electrical performance and efficient, high-yield, cost-effective, defect-free manufacturing.

Almost all seasoned designers have had all three of these facets developed over their careers and know how to make nuanced decisions that play a significant role in the success of their company’s products. So again, managers who assume that anyone can take a PCB MOOC course, read Wikipedia or just start doing PCB layout successfully are not dealing with reality. They are doing their company a disservice with this flawed line of reasoning.

During IPC APEX EXPO 2018, I attended the IPC Designers Council executive board meeting. We were in deep discussion about this very subject and sharing our collective industry frustrations about the lack of awareness and response. As members of this council, we have spent significant time and energy trying to act and raise awareness over the years. One statement made that night has me concerned and I hope it never comes to pass:

“Maybe this has to fail before they all take notice?” Or in the words of Joni Mitchell’s, “Big Yellow Taxi: “Don’t it always seem to go that you don’t know what you’ve got til its gone.”

What I have done in this article, as well as what I have done in prior articles, and what my peers typically do, is just describe the problem in the hopes that someone will hear and get the message. We need to do more than just define the problem—we must define the solution!

I am close to presenting some concepts that could make a significant attempt at defining a solution. So, today, I can join in the chorus of, “We have a problem.” But I will also say, “There is a solution coming, so stay tuned.”

DESIGN007



Mike Creeden is VP and founder of San Diego PCB Design, and an IPC-CID+ MIT Trainer with EPTAC.



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Mentor Preparing for Next-Gen PCB Designers

Feature by Andy Shaughnessy
I-CONNECT007

As Bob Dylan once sang, “The times they are a-changin’.” We’ve all seen it: A new generation of young PCB designers is (very) slowly entering the industry, and the designers we’ve known for years are retiring, or at least talking about retiring.

These millennials are going to be the future of our industry. What does this mean for the PCB design community? How do we attract more of these smart young people to the world of PCB design?

I asked Paul Musto, director of marketing for Mentor’s Board Systems Division, a Siemens business, to explain the company’s initiatives aimed at drawing more students into PCB design. We also discussed the recent movement of electrical engineers into PCB layout, the need for a clearly defined path for students seeking to become PCB designers, and some of the ways that young people are already beginning to revolutionize this mature industry.

Paul Musto: Traditionally, as we all know, most companies had functional specialists; PCB designers, electrical, mechanical, software and signal integrity engineers. Many of these companies, if they didn’t have that level of skill sets, would go to service bureaus or outside contractors and would contract for those kinds of services.

I’m an EE. I graduated from Worcester Polytechnic Institute. I was hired into Data General, a minicomputer company in Massachusetts, as one of a new team of electrical engineers to layout printed circuit boards. At that point in time, they were transitioning from a traditional PCB layout process (hand and tape) to a new CAD based flow and wanted to have electrical engineers working on their PCB layouts. They believed that, due to the complexity and high-speed nature of their boards, EEs would have a better understanding of the fundamental electrical performance of what we’re designing.

Being a recent EE, I quickly realized that I didn’t want to do PCB design as a full-time profession and only lasted about two years

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before moving on to a PCB design software company—which I found fascinating. At this time, EDA software was a booming industry and many exciting developments were being made. I have now spent nearly 30 years in the EDA industry, but haven't designed boards since that point. There's always been this discussion that PCB design is going to shift to the EE, because the engineer has more inherent knowledge about the electrical aspects of the design, but we haven't really seen that take place.

Well, I believe this trend is changing due to market and technology dynamics that are changing things up. One is, as we all recognize, the PCB design specialist community is aging and many are retiring, leaving a shortage. Many long established companies you visit will have PCB designers who you've known for 25 years and are now in their late 50s and 60s.

PCB Design is not a skill set that has been developed and nurtured through the years. Twenty years ago, trade schools and community-based schools offered PCB design classes, and many of them referred to it as drafting, and the person a draftsman. There would be all kinds of opportunities in the industry where people could go and learn PCB design, but many of those outlets no longer exist. It's just not a trade or a skill set that's as sought after as it was back then when you had draftsmen, electronics technicians, and mechanical designers moving into the electronics space.

Today you have a whole new breed of design engineers who are coming into the workforce, with the expectation and desire to do a lot more of the overall design process.

Companies are putting electronics in everything these days and many of these companies don't have the resources to hire specialists. As a result, many outsource various parts of the design to service bureaus, or EMS companies. They're running into problems doing

this because they're trying to integrate these electronics into an intricate electro-mechanical products. It is difficult to completely outsource parts of the design and expect that it will meet all of your electrical and mechanical form, fit, and function requirements. Instead, many companies, especially small and medium sized, are counting on their design engineers to do the PCB layout as part of their development. This requires training engineers to develop a deeper understanding of PCB design—beyond just place and route.

Unless they have proper training, they will not understand all the manufacturing nuances. Placing components on a board and stitching connections between the pins is only part of the challenge. Understanding how placement is going to impact your overall design and mechanical interdependencies, how routing will impact electrical performance, and how decisions on layer materials, stack-up, drills, etc. will impact manufacturing yield and optimization are areas that require experience and training.

Another element to this is that they're not doing PCB design all the time. Their skill sets for doing the PCB design are pretty limited since a typical engineer might use the PCB design tools only a couple weeks, or a couple of times, a year. They're not doing it eight hours a day, every day. Their expectations around usability and functionality are different, causing us to re-evaluate our products as well. I often hear that other tools are "good enough." But "good enough" is only good enough for so long. Those tools run out of steam and lack fundamental power to deal with more complex challenges. The goal of our company is to provide the power of our high end solutions in a product offering targeted for the design, or hardware, engineer.

Shaughnessy: You look ahead, and you have to keep an eye on who's using the tools. What does this shift mean for Mentor?



Paul Musto

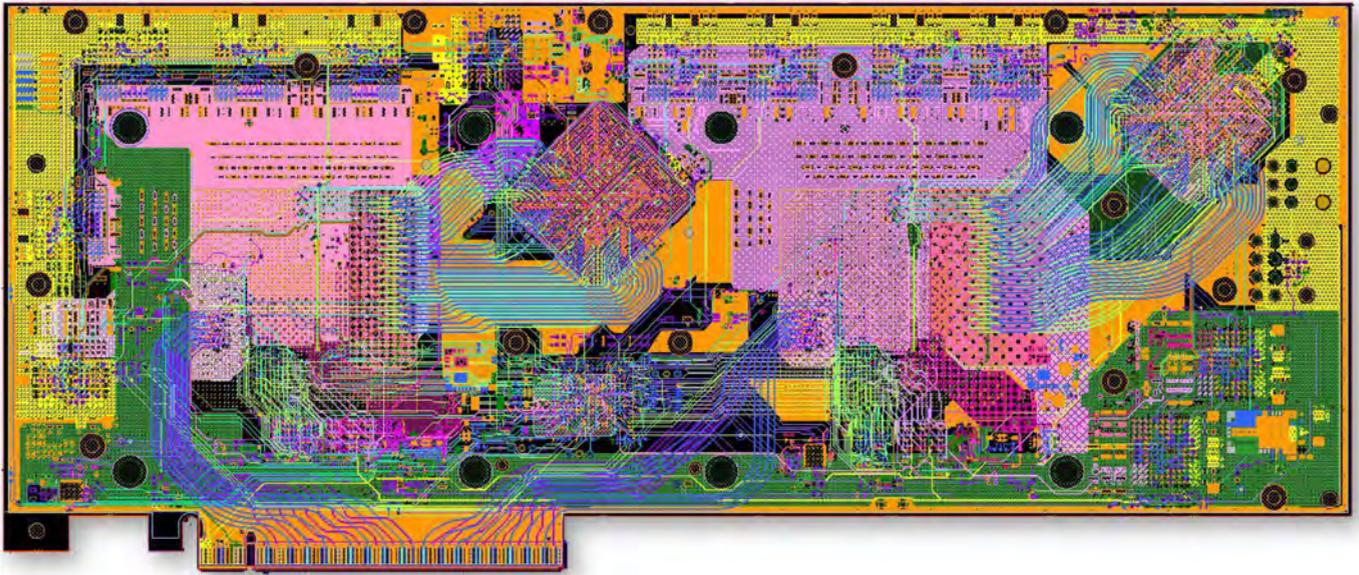


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Musto: When we look at roadmaps, the functionality we have today is incredibly powerful and capable of addressing the most complex design challenges. As I just outlined, we want to bring this powerful functionality to the design engineer in a way that delivers the full power of capability but in an environment that is easy to use, well integrated with other design disciplines, and offers scalability as their needs increase. Understanding that the design engineer doesn't work in the tools every day, they have to be well integrated, consistent use-model and intuitive. I think, however, trading off core capability for usability is detrimental in the long run.

Those are the things that we're looking at. How do we provide a more streamlined use model flow for our customers? If they're going to be "casually" using the tool, they need to be able to get in and quickly get back to a high degree of productivity.

Another initiative and focus area is to move, or shift-left, verification processes directly into the design tool itself, enabling the designer or engineer to catch potential issues much earlier in the design flow. As an example, we acquired a company, Valydate, about a year and a half ago. They provide the ability for full schematic verification using electrical model-based elements. It's completely different than what's been done in the past with schematic verification. Xpedition Valydate schematic integrity

analysis is performed in parallel with design capture, with errors highlighted directly in the schematic, eliminating the need to do tedious manual checking that is often done today. We are also doing the same for our entire suite of verification products, such as DFT, DFR, signal/power integrity, and DFM.

DFM is a prime example of an area that is unfamiliar to the engineer, since an engineer using a PCB design tool a few times a year is just not going to have the knowledge to understand the full set of manufacturing requirements.

Shaughnessy: You said that EEs might not understand manufacturing. I'm hearing stories about some companies that will hire EE grads, maybe top of their class, and find that they don't know much, if anything, about PCB design. Is it just a different skill set?

Musto: Definitely. PCB design is a skill set that requires knowledge of many areas in order to do well. As a result, I think we're going to have to maintain a PCB design specialist function in the broader community. I believe they're going to be driven more toward consultant roles to deal specifically with these kinds of issues, because a design engineer, even if you train them, doesn't really have a focus in these areas. Engineers care about getting a functional product at the end of their flow, so the intricacies of PCB fabrication is not on their "care-about"

list. “How do I get the design done, tested, validated, and I know that it’s going to work when it gets manufactured?” That’s their focus.

We’ve been out talking to universities and working on a number of different initiatives to drive improved education. Here’s in lies another challenge. Back 20 years ago, you could go to a trade or two-year engineering tech school, and they would have a PCB design fundamentals class as part of their curriculum—or would be very interested in having it. This has waned through the years and is now difficult to even find. Today, the IPC manages a training program to certify PCB designers, but even that has limited reach.

The focus today has shifted to the engineering departments of universities. However, when you go to a university’s electrical engineering department and talk to the faculty, they’re not interested in teaching a PCB design class. They are more interested in enabling their students to use PCB design tools to do classwork, or to do a project. That’s a challenge, as well, because we’ve traditionally taught full classes focused purely on PCB design. That’s not really what they want to do. They want to have it integrated into the curriculum.

We’re working with a couple of the universities in a couple of different ways. One is the integration of PCB design principles into an existing EE curriculum, and we’re also piloting kick-starter classes. At one of the universities, we’ll hold a one-hour class on weekday nights. They’ll do PCB design principles, a kind of kick-starter program for engineers who want to learn a little bit more about the PCB design process. We’re going to have a series of those modules with the plan to offer a full MOOC (massive open online course) and on-demand video channel on PCB design principles by the end of the year.

Shaughnessy: That sounds like a good way to present the content. Plus, you’re working with college kids. You almost have to go look for them, because they’re not going to find us.

Musto: You’re right. These young engineers are not focusing on PCB EDA software and,

as such, they are difficult to reach. With the shifting demographic, we’ve also been looking to hire new industry entrants to represent the new wave of design and engineering professionals. This has been a difficult challenge.

Although difficult, we have been successful in finding candidates to fill these roles. We’ve recently hired an engineer who fits the bill completely—one that does electronics design, PCB layout, mechanical, and software—a true multi-disciplinary engineer. The fact that he has also worked with many CAD/EDA applications is also a major plus.

Shaughnessy: Speaking of degree versus non-degree, I’m starting to hear about companies that won’t even consider hiring a PCB designer who isn’t a college grad. Some of these companies are full of non-degreed senior designers, but as they retire, they’re being replaced by someone with a degree. They just have to check that box. On the other hand, if it takes a degree to be a designer, maybe this will get it into the college kids’ heads a little earlier.

Musto: To this point, I received an interesting email last week. Long story short, there was a gentleman in his early 50s, and he was looking for recommendations for engineering schools. His company was looking for a university degree as a requirement for their PCB designers. I’m thinking, “Wow, that’s a rough situation to be in.” To be honest with you, I’ve been in conversations where I’d scratch my head and say, “That’s not practical.”

To be honest with you, I’ve been in conversations where I’d scratch my head and say, “That’s not practical.”

At the end of the day, PCB design is an electronics function, and you should have some understanding of the electrical aspects of

doing design. There's also another skill that's involved here. A lot of people invest their lives in becoming a great forward thinking PCB designer. To expect an electrical engineer to do that is not realistic. I'm not saying it's impossible, but I just don't think that, 10 years from now, you're going to see even large companies with CAD teams of PCB designers who are EEs. I think that the function is going to be dispersed or disaggregated from the centralized function into project teams, where it's going to be shared amongst the engineering folks. This said, there will still be a need for PCB Design professionals to ensure design integrity is met and all manufacturing requirements are fulfilled...without this, ECO's will become more commonplace.

Shaughnessy: Then there's China, graduating hundreds of thousands of electrical engineers each spring. Do you have any insight into the growth of PCB designers in Asia? Do you think that's going to be a threat? The US would hate to lose our dominance of PCB design.

Musto: China is definitely different to what we have been discussing. They're graduating large quantities of electrical engineers and, because the pool is so large, we are seeing a larger

number of PCB design professionals with EE degrees.

In North America, engineering students are more interested with becoming the next entrepreneur or working on major electronic product innovations. In this spirit, they have greater aspirations than working in just one functional discipline. As stated before, they are diversifying and focusing on many elements of the product creation process, PCB design just being one of them.

IPC is looking at this too. It'll be interesting to get their perspective. From my understanding, they are interested to reinvigorate the PCB design trade through education. I think that there's still going to be a place for this type of education for individuals who want to advance their knowledge of PCB design and manufacturing. Good industry PCB designers will continue to demand a premium, sometimes more than the EE's, for their comprehensive understanding of taking a design all the way through to manufacturing.

Shaughnessy: You mentioned training. A lot of U.S. companies still don't understand is that it's in their best interest to send their designers and EEs to classes at DesignCon, PCB West, or APEX, and they shouldn't have to take vacation days to improve their skill set. When it comes to training, OEMs in the U.S. are stepping over a dollar to pick up a dime, and I wonder if it's that way in other countries.

Musto: I agree. Here's an example: We conduct PCB seminars around the world each year. In North America, we're happy to get 30-40 people in the room. In the Pacific Rim, we could run the same exact session and have 200 people in the room. It's just unbelievable. In the Pacific Rim, there's a bigger desire to attend these kinds of events and is supported by their companies. We do find that this changes when

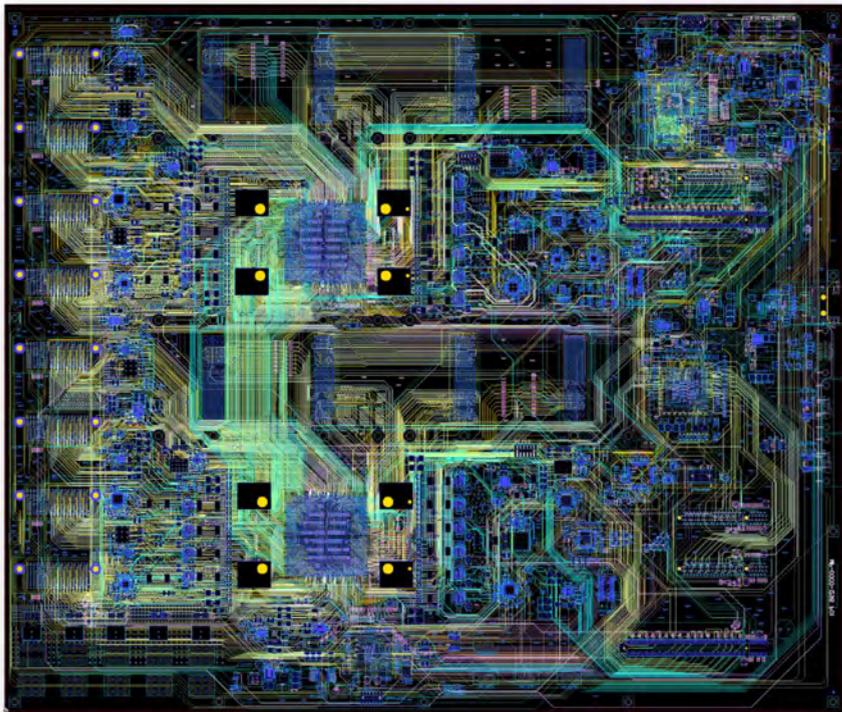


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an outside industry speaker comes in and presents an industry topic of interest. No matter where, we tend to draw some pretty large crowds.

We have had companies approach us, and say, “Hey, we need your help to go to a local university and develop a curriculum for them.” Their thinking is, “We’ll just use the local university to create a PCB design curriculum so we can produce PCB designers.” When you go to the university, they are always interested but typically not interested in a dedicated class on PCB design in their curriculum. They would rather PCB Design be integrated as part of the overall engineering coursework.

Our approach is to have kick-starter modules that can be self-taught, or taught through mini sessions, and then have actual PCB design principles integrated into the EE curriculum. For instance, we’re working with a university located near one of our main offices. They teach a class on signal integrity principles in PCB design and Mentor’s working with him on integrating our tools into his class.

Ultimately, all of this will transform into a complete set of learning materials targeted for the engineer. My recommendation to companies looking for young designers would be to work with your local universities and encourage them to put these elements of training into their programs. Maybe it’s my own personal

past but I’m reluctant to say, “Oh, yeah, just go in and start training your EEs to do PCB layout.” This is potentially taking somebody’s career and pushing them down a singular path, which I think is going to be problematic.

Shaughnessy: Now, these kids have had a cell phone since they were five, so they want the tools to work right out of the box. They turn it on, and they want it to work. Waiting days for tech support to call back isn’t going to cut it for them.

Musto: You hit the nail on the head. This is a major shift, and disruption, to classical EDA tools.

It’s a completely different mentality toward using tools today. Since many engineers do not use the tools on a constant basis, usability is now a top priority. It’s not that usability isn’t important for everyone, but professional PCB designers use the products day in and day out so they learn to get the most out of the flexibility and power of the tools. Sometimes power and flexibility come at a cost of usability. There are many examples of this—even in consumer software. For example, for photo editing, you can use Photoshop Elements for those who are not professionals and Photoshop CS for those in the profession. Photoshop Elements provides much of the power of CS but in a much simpler UI. We need to do the same. This has the inherent benefit of scalability as well. Scalability of software tools is also of major importance since, eventually, more power will be needed to handle more complex design challenges. Scalability is also critical in large enterprise companies where designs in the engineering domain feed into a larger system design. In this case, there are also the benefits of data sharing, such as libraries, re-use modules, and general infrastructure.

Shaughnessy: We keep hearing about millennials being so lazy and wanting a participa-

tion trophy, but I've seen some real go-getters lately, including my young co-workers.

Musto: That's an interesting point. Most of these really small companies have small teams of innovative, sharp, bright young engineers, and they're just engrossing themselves into their entire product design, which is great to see. These engineers are getting involved in every aspect of product design, from the hardware, software, to the mechanical. I've come across electrical engineers who also do mechanical and software. This is changing how our end customers use our products and the expectations they have. Now to your point about millennials, they are not lazy, they just have completely different expectations from the traditional EDA user community, and quite frankly from the traditional EDA suppliers. They want to get their info digitally, on-line, through active YouTube channels, pod-casts, live chat forums, they expect to be able to find anything with just a mouse click, without signing up or logging in.

I think we all recognize that a tremendous amount of innovation is coming from the start-

up community, usually driven by young engineers with a dream, a vision, a passion, and I always talk about this in my presentations. I specifically talk about the automotive sector, the electrification of cars, and autonomous automobiles. I was reading an article about 300 new start-up companies created in the US last year just to service the autonomous and electrified vehicle ecosystem. The large OEMs and Tier 1 companies are also acquiring many of these companies for their innovation which is influencing the way they develop and design new products. One way or another, these start-ups become this critical element to the broader picture.

We've been talking about the transition of PCB design from PCB designers to electrical engineers for 30 years. I think we're right on the edge of that really happening...but not without the support of the PCB design professionals currently in the industry.

Shaughnessy: Great. Thanks for your time today Paul.

Musto: Thank you, Andy. **DESIGN007**

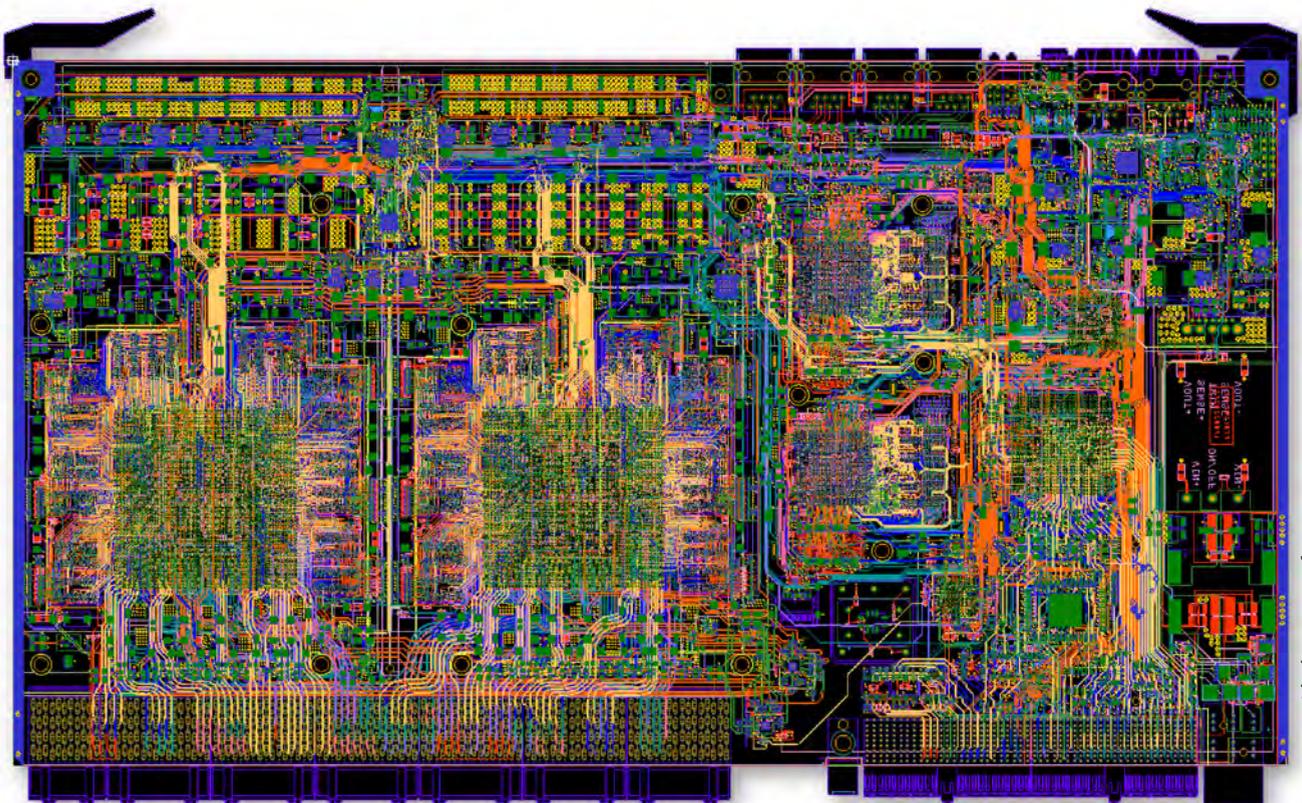


Image provided courtesy of Mentor

Where Have All the Designers Gone (and Who Will Be Taking Their Place)?

Tim's Takeaways

Feature Column by Tim Haag, CONSULTANT

“Where have all the designers gone, long time passing?”

With apologies to Peter, Paul & Mary, the answer is that a lot of us are still here. Yes, many designers have retired, and sadly, we've seen some pass away, but there are still many seasoned professional PCB layout designers hidden in plain sight and working away.

Questions like this are often grouped together with questions about what has happened to our industry. All together, they are usually part of a larger discussion about “the good ol' days,” and people lamenting how things just aren't the way they used to be. But we have to ask ourselves, “Do we really want things to be the way that they used to be? Do we really want to lay out high-density routing using tape and dollies on a light table?” I certainly don't. So I would suggest that the changes we are seeing

in our industry today are a good thing.

Everything in life goes through changes. If it's living, it's growing, and if it's growing, it's changing. We should all be more worried about time when there aren't any changes in our lives, or our careers, for that matter.

Have you ever worked for a company where everything was the “same old same old,” and nothing ever changed? I've been there, as I'm sure many of you have too. That gradual descent from a growing company to a stag-



Figure 1: Looking cool in 1978. Looking cool was easy for me 40 years ago.



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nant one can easily turn into a death spiral as an organization slowly withers and dies, ultimately leaving you looking for work elsewhere (and forcing yourself into change).

One of those changes will be growing older in our careers, which brings us back to our starting point. Where have all the designers gone? As time moves on, we will hand the reins over to the next generation of PCB designers. Fortunately, this next generation won't be going at it alone. They can build their own career paths on a strong foundation of PCB design techniques and methodologies that have been laid down by all the designers preceding them.

I am proud of the integrity and work ethic that PCB designers have become known for. PCB designers are the type who will keep working at a task because it isn't the way that they want it, or there's a deadline to hit. I've known designers who have spent the night working out a problem in their layout because the job had to be done by morning. I've also known designers who have refused to sign off on a job to meet a schedule because they knew that something wasn't quite right. It's traits like these that have helped designers to earn their highly regarded reputations of quality, and that is just one of the great things that we will be able to pass on to the next generation of PCB designers.

And we have a lot to pass on to the new designers. We must stress the importance of understanding the roots of our industry and why this design knowledge is important. I have worked with many designers who don't understand anything about the output of their design files. They go through a procedure, hit a series of commands, and presto: The design files are all wrapped up in a neat little zip file ready to go out to the manufacturer. That's all well and good, until something breaks or a manufacturer has a spe-

cific question. It would be a great thing to make sure that the designers of tomorrow understand what a Gerber file and an aperture list really is. Output files will eventually all morph into the next best file format and processes, but it is still a good idea to know where we have come from and why those files do what they do.

We have to help the new designers understand the job completely, from design through manufacturing. A lot of new PCB designers know how to design a printed circuit board, but they have very little idea how that PCB will be fabricated and assembled. Because of that, they may not make the best design choices when it comes to layer stackups, clearances, and design rules in general. I think that we have a great responsibility to help new designers to fully understand what happens after the Gerber files are created. At the very least, it would be a great start if we could convince some of these beginning designers to give their manufacturer a call just to get acquainted.

Same, but Different

How will the designers of tomorrow be different? When I started in the industry, the designers I learned from were the last of designers who had sketched their designs out in colored pencils before taping

them up for a process camera. These guys were artists, but after a while, those of us from the computer generation took over for them. There wasn't much in the way of formal education for a PCB layout designer back then; usually we came from a background of mechanical drafting or working as a board technician.

Today the requirements of design have changed again. We are seeing more and more PCB designers who are doing the full PCB design, from the schematic all the way through layout. Because of this, designers



Figure 2: Playing laser tag in 1994. Designers aren't geeks, are we?



Figure 3: With my grandson recently. Is he going to be a PCB designer when he grows up?

entering the field of PCB layout today often have a background in electrical engineering. Some would complain that this sort of change is unnecessary and unfortunate, but I disagree. Is it any different than when those of us with computer skills stepped into the role of PCB designer instead of using colored pencils and tape? Remember that change encourages growth, and growth causes more change.

On Father's Day, I received a gift of fruit dipped in fancy chocolate. While I was trying to convince my wife how healthy this was for me (it's fruit, right?), she rolled her eyes and was kind enough not to comment on how fast I consumed it (less than a day and a half which must be some kind of record). But the other gift that I received is more pertinent to our topic: a wireless video doorbell. How cool is that? It simply connects to my Wi-Fi, and now we get a notice on our phones when someone rings the doorbell.

For a long time we have wanted a security camera for our front door. But the thought of positioning, wiring, and adopting it into our way of living just hasn't been something that I've wanted to take on. The funny thing is that I've been designing cool electronics for my whole career, yet I was unable to imagine just how simple this could be.

I didn't need to install a complicated security camera system; I just bought this simple

and relatively inexpensive little wireless doorbell instead. It gives me the video feed from a camera straight to my phone, a two-way intercom, and it can draw power from the old doorbell circuit to charge its battery. I can even pay a low subscription fee to a cloud service if I want to record the video.

The reason that I told this story is that it never occurred to me, someone with decades of experience in the electronics industry, that something like this could be done. It did occur to someone though, and they went out and made it happen. That kind of inventive entrepreneurial spirit is what we need in tomorrow's PCB designers, and we need it today.

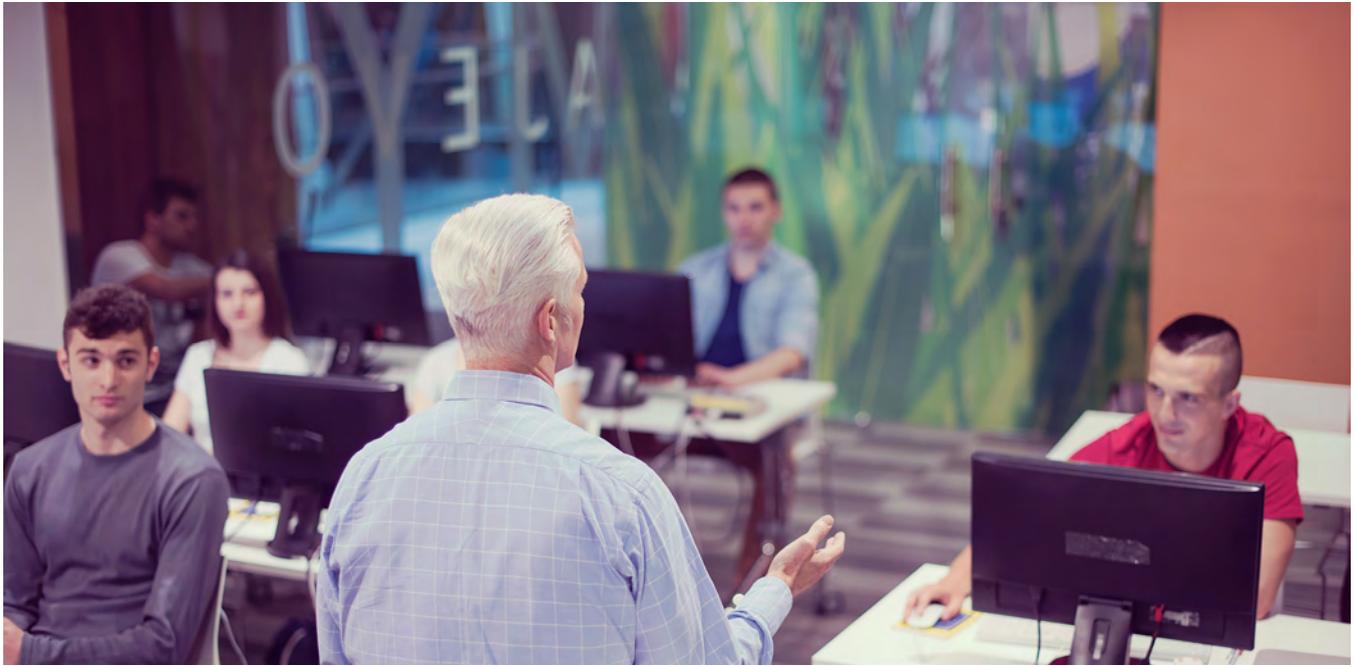
So, on one hand we have a bunch of folks out there who have been designing printed circuit boards for years and years. They've got a rich legacy of skills, experience, and integrity that only comes with doing their jobs for a long time. Then, on the other hand, we have a bunch of new folks coming into the field of PCB design that have the latest knowledge, ideas, and education. You see where I'm going with this don't you? Let's get all of these people together.

The changes in our PCB design community shouldn't generate depression and fear. Instead these changes should motivate us to encourage and learn from each other so that we can all do our jobs better and create more and more really cool next generation technology. Change encourages growth, and growth causes more change.

It really is a great cycle of life to be in. Excuse me. My phone just lit up announcing that "Someone is at your front door," and I'm really hoping that it's another delivery of chocolate-covered fruit. **DESIGN007**



Tim Haag is a consultant based in Portland, Oregon.



In With the **NEW** at Cadence

Feature by Andy Shaughnessy
I-CONNECT007

The next generation of PCB designers is coming—slowly, but surely. What will this new group of designers mean for EDA vendors like Cadence Design Systems? I recently interviewed Dan Fernsebner, product marketing group director and a veteran EDA guy, and Bryan LaPointe, lead product engineer and representative of the younger generation. They discussed the next generation of PCB designers, some of the best ways to draw smart young people into this industry, and why the PCB designers of the future may need to have a college degree just to get an interview.

Andy Shaughnessy: Bryan, how did you get involved with Cadence?

Bryan LaPointe: Cadence was a bit of a long journey for me. I started in the design world, which I kind of stumbled into. After a few years of leading designs, I started putting together presentations and winning awards at different

seminars and conferences, such as CDNLive and PCB West. From those, I started getting a little exposure and saw that a position opened up here for product engineering and I made the jump.

Shaughnessy: What was your degree in?

LaPointe: I have a bachelor's degree in forensic science. Totally unrelated.

Shaughnessy: Everyone has a different path.

LaPointe: Right. I worked in the physical sciences for a little while in the labs, something more related to my degree. Then, I ended up stumbling into an internship that taught not only PCB tool basics, but terms, technologies, and everything. This eventually led to a full-time designer position and being a bit of a team lead. That all cascaded from there.

Shaughnessy: When you were in college, were you aware that there was this field called circuit board design, or was that later?

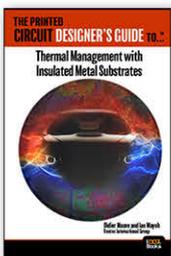
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LaPointe: No, I was totally oblivious to it. PCB design is so underexposed. People don't really know it exists. The people who use all these electronics just take it for granted that they hit a button and something turns on, but the whole



Bryan LaPointe

subset of the design world goes unnoticed because people think of the product, but they don't think of how it actually gets there. I didn't even know PCB design was a thing. I knew PCB assembly existed—obviously the phones and such have to be put together—but no, I never made the connection that somebody actually had to connect all those little parts together.

Shaughnessy: Dan, as the wise, elder statesman here [laughs], are you seeing more young people getting involved in the industry?

Dan Fernsebner: Absolutely. We live in this revolutionary period, in terms of the age of IoT. The explosion of electronic hardware is just incredible. I think a lot of that has to do with the accessibility to design tools, the reduction in cost of manufacturing and components, and the internet in general, in regard to providing information and enabling young designers to experiment.

I think it's interesting what Bryan said. Even when I came up through college, PCB design or layout wasn't something that was necessarily taught—it was something you learned through trial and error and co-op work. Learning PCB layout is becoming harder for this next generation because a lot of the older designers are now retiring, and they are the ones trying to pass the torch.

Because of that, I almost feel that expertise is being lost in the mix. Because of this trend, we are being asked for classes—not about our software—but just around PCB design itself.

Shaughnessy: Does Cadence have relationships with colleges?

Fernsebner: Yes, Cadence has a program called the Cadence Academic Network, which is focused on promoting the proliferation of leading-edge technologies and methodologies at universities known for their design and engineering excellence. Not only do we promote collaboration between academia and industry, but we also provide schools with Cadence software and sponsor a number of academic clubs run by universities and the students themselves. To acquire new talent, university recruiting is also an important part of the program so it's definitely something that we're pretty in tune with.

Shaughnessy: Do you think you'll have to change the tools to accommodate the next generation of designers? These young people don't remember ever not having a phone. Designers our age are willing to wait for a patch to fix a software problem, but the young people want it to work now.

Fernsebner: Yes, agreed. This new generation, Generation Z or the I Generation, is the first generation that grew up with a smartphone. I'll let Bryan speak to some of the interface stuff because he and I have been working pretty closely and based off of his experience being a young designer, he definitely has a lot of input in that space.

LaPointe: It's a really interesting paradigm. When CAD tools first came out, they were on different systems and technologies. Now that there are so many available at such different price points and accessibilities for training, it's very simple for somebody to pick up the tool, and if it just doesn't feel right or work right, it's very easy to go find another one that does—especially for the younger crowd. There's more of a focus on first-time use, ease of use, and instant gratification—even things as simple as control-C. If control-C doesn't copy when you open up the tool, it immediately puts something in their heads that something's not quite right.

Whereas for the people that grew up with the tool, they might have their own crazy combinations for copying, but it's definitely different. It's like you said, growing up with the technologies, you get so ingrained with things that feel natural and aren't cross-platform and cross-tool. The younger crowd is expecting that. They almost feel as if they're entitled to it. If it's not, it almost feels like we're shorting them.

Shaughnessy: Designers years ago called their EDA tools "job security" because they were Unix tools and no one else in the office could just jump on the tool and start designing. It's not like that anymore.

LaPointe: No, in so many startups and young companies, there really isn't that job security or that guy who is trying to be the wealth of knowledge.

Some of these people need to be able to pick up the tool, make their product, and get a prototype for their customers. They can't afford months and months of training trying to learn interfaces and technologies. They really have to be able to install this tool, get it up and running, and work on their projects immediately.

Shaughnessy: Right. Among your classmates and friends your age, are any of them in this industry or any sort of electronics careers?

LaPointe: Some of them are. When I ended up getting into the industry I started talking to my friends about what I do, what technologies there are, and what the industry does. A few of them did take interest and ended up taking internships or positions elsewhere. They've had the same trickling effect. They've told some friends who've since applied.

Word of mouth, at least for me, has seemed to be a good way to get people into the indus-

try. I don't know how it works for everyone else, but it's definitely the easiest way to spread the word.

Shaughnessy: Did Cadence require a college degree for your position?

LaPointe: They did, a combination of experience and a college degree. Obviously, with enough experience, that counters out that degree, but yes, they do. They want to see a wealth of ability and knowledge, a bit of a balance, and obviously real-world experience.

Shaughnessy: Where'd you go to college?

LaPointe: The University of New Haven in Connecticut.

Shaughnessy: OK. You know, a designer friend of mine was out of work and he ended up finding a job, but a lot of managers told him, "You're ineligible because you don't have a college degree." It seems like they're starting to want designers to have some kind of degree now, which is a total sea change from before because most of the senior designers that I know have maybe six weeks of community college.

LaPointe: Yes, that's definitely true. The environment that I was designing in, the majority, if not nearly all of them, had high school degrees. They didn't have a formal college education. They weren't EEs, though one or two were EEs who actually switched

to design because they liked it so much. Part of it is because the pace that technology has moved creates this really big gap where if you bring on somebody without a degree, the curve to get them up to speed is almost too great.

If you come on with that EE experience, you've got a basic understanding of the ter-



minologies and components. You still need to learn how to create the traces and push some parts around, but a lot of the understanding of it is framed out, if that makes sense.

Shaughnessy: I'm just wondering if all of this hype about autonomous cars, 5G, virtual reality, and cross reality are helping attract more young people to our industry.

LaPointe: Yes, I think it has. Again, purely through osmosis, where if you have this startup company and they're working on an autonomous car, even if you went in with the intention of being an EE, at some point one of you has to switch over and start doing the PCB design. All these newer companies and technologies push people into the design roles.

Shaughnessy: Dan, is your background in engineering?

Fernsebner: Yes, I graduated from the University of Massachusetts Lowell with an electrical engineering and computer science degree, so the EDA space was a perfect space for me.



Dan Fernsebner

It is a good cross between software and hardware.

Shaughnessy: Did you hear anything about circuit board design when you were in college?

Fernsebner: No, I mean obviously you get exposed to it when you're there, but before that, it

was probably one of the furthest things from my mind. It's not something that they teach, and from my understanding today, it's still not taught. I would think in the future schools would start looking at their curriculum and start making adjustments.

You can see some of that now where you have the mesh of electronics and mechanical.

Schools are now offering degrees in mecha-tronic engineering. Hopefully PCB design is something that will eventually become part of the curriculum, but who knows.

Shaughnessy: I think it's just a matter of reaching out and looking for these kids. I liked what IPC did at APEX this year; they invited high school kids from San Diego to attend the trade show, walk around, talk to everybody, and meet some of the people in the industry.

Fernsebner: Things like that are great, as well as the Maker Faire, which is worldwide and quite large. Even now, a lot of the toy companies, like Lego and others, are really starting to promote electronics in different forms.

Shaughnessy: Maker Faire is really something. We have one employee who just got out of school a few years ago and he already knew how to solder a circuit board because he'd attended Maker Faire.

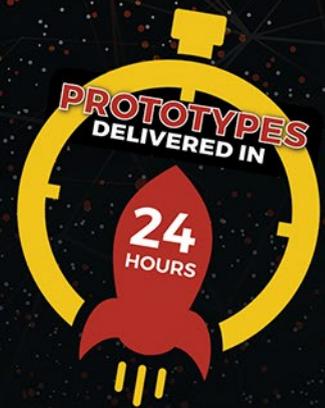
Fernsebner: One toy company called littleBits lets you assemble circuits using magnetic connectors. I think a lot of this is making electronics more relevant much earlier on.

Shaughnessy: Is requiring a degree really a blessing in disguise? Designers now deal with signal and power integrity and EMI problems where some engineering and theoretical knowledge would probably be a benefit.

Fernsebner: I agree, and I think that's probably why a lot of companies are asking for engineering degrees because I think back in the day, a lot of mechanical designers and draftsmen became PCB designers. Back then, it was really about the artwork and how good you were at detailing that artwork.

It's becoming much more of a science. The reality is, it's only going to get worse. We're just talking about 5G and DDR5 now, but in two years we'll be talking about 6G, DDR6, and so forth. It very much seems like nowadays the bachelor's degree is a commodity in the marketplace, where having a bachelor's degree in

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Shaughnessy: Wow. That's a whole new "how I got into PCB design" backstory.

LaPointe: True story. It can be as crazy as that. The man had his own little design service and he needed some help, so he asked his mailman if he wanted to be an intern and the mailman said, "Sure." Now, he's a designer.

Shaughnessy: When you got to Cadence, did they send you through classes on their software or did you already know about their tools?

engineering before was unique. It meant that you spent all this academic time to really put yourself together. These days, having a bachelor's degree is just another tick in the box.

Finding someone without a bachelor's degree, sure you could do that, but the competition in the market space means that you could just as easily find someone with a bachelor's degree, so why not make a degree a requirement? Plenty of the people who graduated with it are struggling to find jobs or they're competing against hundreds of other people in their fields. STEM fields and education is definitely changing.

Shaughnessy: One thing I was thinking is that maybe this having an actual path to a job will be a really good thing. There has never been a real path to this job, so if you're a high school guidance counselor, design is not even on your radar. Maybe if college becomes a requirement, these counselors will start spreading the word because there's decent money to be made in this field if you know it exists.

LaPointe: That's a good point. A lot of the people who I started working with were originally in drafting or something else. One guy was actually a mailman. He showed up to deliver mail to somebody's house and they offered him a trainee position as a PCB designer.

LaPointe: I was actually a very heavy user of the Cadence tool set before coming in, so I was very familiar with the layout tools, specifically Allegro and OrCAD. I did have to do a little bit of learning on my own for some of the schematic and simulation tools, but we had internal training and there were external resources everywhere. By and large, I already knew what I was getting myself into.

Shaughnessy: Very cool. How do you think all of these newcomers to design are going to affect Cadence and other EDA vendors?

LaPointe: I don't know about the company, but I think the industry's going to have to learn to make changes. As Dan said, when dealing with the newest generation, I don't think you can do things the way they've always been done. That's not just for us at Cadence; that's going to apply to everybody.

I think it will have to be incremental for everyone because nobody has the resources to immediately jump in and change the whole industry overnight, but somebody needs to start paving the way.

Shaughnessy: I talked to one company that has a lot of millennials, and they said one thing really helped—having a dunking booth so the kids can dunk the older people. Salary isn't as



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important to them. Since they got a great job right out of school, they figure they can quit and jump right into a better position, but they can't find a better job and ask for their old jobs back. They call them "boomerangs" and they rehire some of them, because it's 4% unemployment now and it's hard to fill open positions.

LaPointe: That's another problem, for sure. The retention rate in the industry is pretty low and the newer generations come out with this expectation that they're going to get this great job, it's going to be exactly what they were taught in school, and they're going to apply all of the things they learned. They get into the real world and see that this company might have their own processes and procedures, and maybe this technology doesn't really work that way. They go to some other company thinking it'll be better. Then they get there and realize, "Oh, this isn't that much better if at all."

Shaughnessy: Do you have anything you want to add?

Fernsebner: I can't think of anything off the top of my head, but it'll definitely be interesting. I think that for the next generation of designers, Bryan and I are constantly looking at new user interfaces and models because all of those dynamics are changing.

Shaughnessy: Yeah, it's funny. Years ago, EDA tools had the same GUI for years, maybe decades, and now they get a refresh of the interface every so often.

LaPointe: Yes, I've been told stories, and of course I haven't been around long enough to experience this, but I've heard stories of these senior designers almost losing their minds over just changing an icon here or there or moving a toolbar around. But things need to be optimized and streamlined, even if that does mean making changes. Of course, there's that balance where you don't want to upset the existing users, but you can't neglect the up-and-coming users.

Fernsebner: I think the other consideration is that this generation was born on their smart-phone, and now there's an expectation that they can take advantage of that mobile technology in different ways, so that has also changed the way we look at develop new user interfaces.

Shaughnessy: Thanks for your time.

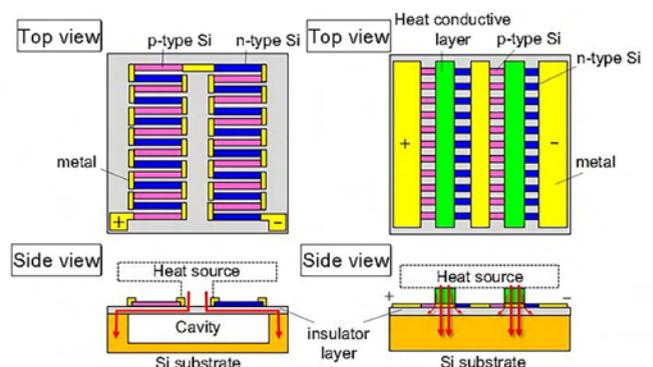
Fernsebner: Great. Thanks, Andy. **DESIGN007**

Opening Up a Pathway to Cost-effective, Autonomous IoT Application

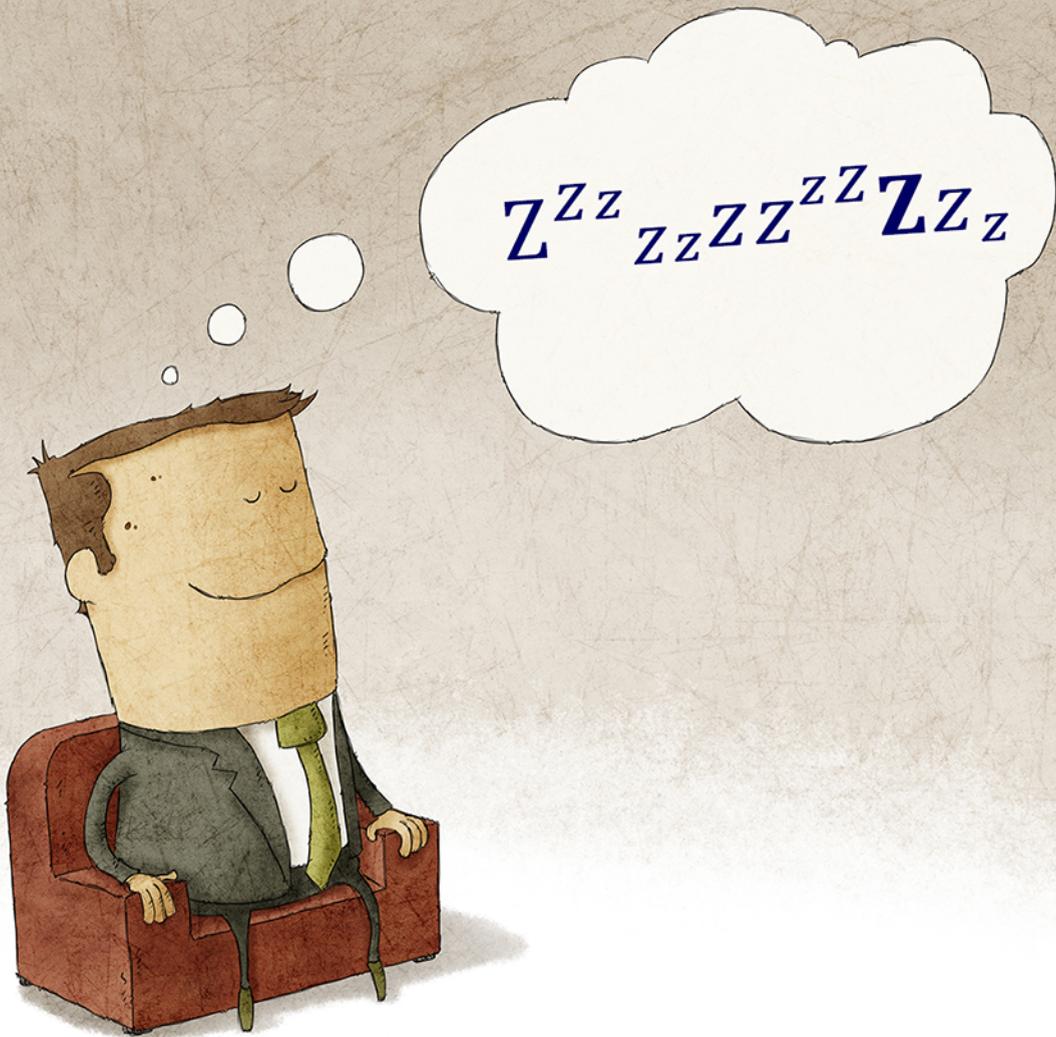
Due to its relatively low thermal conductance but high electric conductance, silicon nanowires have emerged as a promising thermoelectric material. A team of Japanese researchers from Waseda University, Osaka University, and Shizuoka University designed and successfully developed a novel silicon-nanowire thermoelectric generator, which experimentally demonstrated a high-power density of 12 microwatts per 1cm², enough to drive sensors or realize intermittent wireless communication, at a small thermal difference of only 5°C.

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PCB007 Highlights



The Augmented World Expo: Go XR or Become Extinct ▶

Now on its ninth year, the Augmented World Expo (AWE USA) is perhaps the largest event for professionals focused on providing science fiction-like abilities through XR (cross reality) and associated wearable technology. This year's event showcased over 100,000 square feet of exhibit space and featured numerous presentations and discussions covering topics ranging from the latest and greatest uses and devices for XR to the business of marketing and monetizing it.

The Institute of Circuit Technology Annual Symposium 2018 ▶

ICT technical director Bill Wilkie is well-known for choosing notable venues for Institute of Circuit Technology events, and his choice for this year's Annual Symposium was the National Motor Museum, located in the village of Beaulieu in the heart of the New Forest, a national park in the county of Hampshire in Southern England. The region is known for its heathland, forest trails and native ponies.

The Shaughnessy Report: Got Flex? ▶

Welcome to the first issue of Flex007 Magazine. This new quarterly magazine is dedicated to flex system designers, electrical engineers, flex PCB designers, and anyone responsible for integrating flex into their products at the OEM/CEM level.

Standard of Excellence: Making Your PCB Fabricator Your PCB Partner ▶

Are your PCB needs exceeding your vendor base's capabilities? Do you feel that your suppliers are no longer able to keep up with your PCB needs? Are you finding an issue locating alternate sources for PCBs due to the consolidation of the larger shops in our industry? If so, you are not alone.

ACE's AccuWrap Simplifies Multiple Sequential Laminations with Blind Vias ▶

At DesignCon 2018, I spoke with James Hofer, general manager for Accurate Circuit Engineering, a quick-turn fabricator based in Santa Ana, California. James gave me a preview of AccuWrap, a new type of processing technology that lets designers reduce the amount of copper during sequential laminations while still meeting IPC specs, which should be of great interest to RF designers.

APCT Moves into Rigid-Flex with Cartel, Cirtech Acquisition ▶

When I spoke with APCT President Steve Robinson a year ago, he said he was interested in adding flex and rigid-flex capabilities, and working closely with designers and engineers. With the recent acquisition of Cartel and their subsidiary Cirtech, APCT now has a flex and rigidflex facility, along with military and aerospace certifications. At DesignCon 2018, I asked Steve to discuss these acquisitions and what they mean for APCT and their customers.

Candor is Breaking Boundaries with Flex-Core Boards ▶

Sunny Patel, Candor's technical sales manager, remarked about the accomplishment, "We are pushing the limits on our flex manufacturing, going for much thinner laminates and different material stiffeners."

It's Only Common Sense: Producing the Greatest Products Possible ▶

Laurene Powel Jobs, wife of Apple Co-Founder and CEO Steve Jobs, was once quoted describing how her husband and legendary designer Jony Ive would spend hours discussing corners. Yes, that's right—corners.



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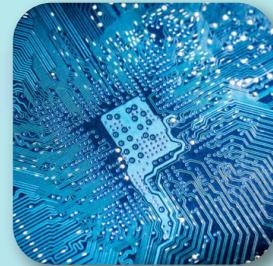
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Crosstalk Margins

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by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

What is an acceptable level of crosstalk? That depends on the technology being used, and this level has changed quite dramatically over the years, going from TTL logic devices to today's high-speed Gbps devices. The amount of power a CPU uses, and thus the amount of heat it dissipates, is the product of the voltage and the current it draws. The trend is towards lower core voltages, which conserves power. But, reducing the core voltage also reduces the noise margin. In this month's column, I will delve into the threshold of acceptable crosstalk and how to mitigate its impact on high-speed designs.

Crosstalk is caused by the coupling of the electromagnetic fields. Electric fields cause signal voltages to capacitively couple into nearby traces. Capacitive coupling draws a surge of drive current, which causes reflections on the transmission lines. Whereas, magnetic fields cause signal currents to be induced into nearby traces. Inductive coupling produces ground bounce and power supply noise. Crosstalk falls

off rapidly with the square of the distance and the degree of impact is related to the aggressor signal voltage, available board real estate and thus the proximity of signal traces. Crosstalk can appear as either far-end, forward crosstalk (FEXT) or near-end, reverse crosstalk (NEXT).

Fortunately, synchronous buses, as typically used for parallel data signal transfer, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking. The crosstalk must be specified during the setup (t_s) and hold (t_H) window at the receiver. During this interval, the crosstalk must never drive any valid signal across the receive threshold to the opposite logic state. So, providing the receiver waits sufficiently long enough for the crosstalk to settle, before sampling the bus, the crosstalk has no impact on the signal quality at the receiver. If the crosstalk arrives during the signal transitions (Figure 1), then its only impact is jitter

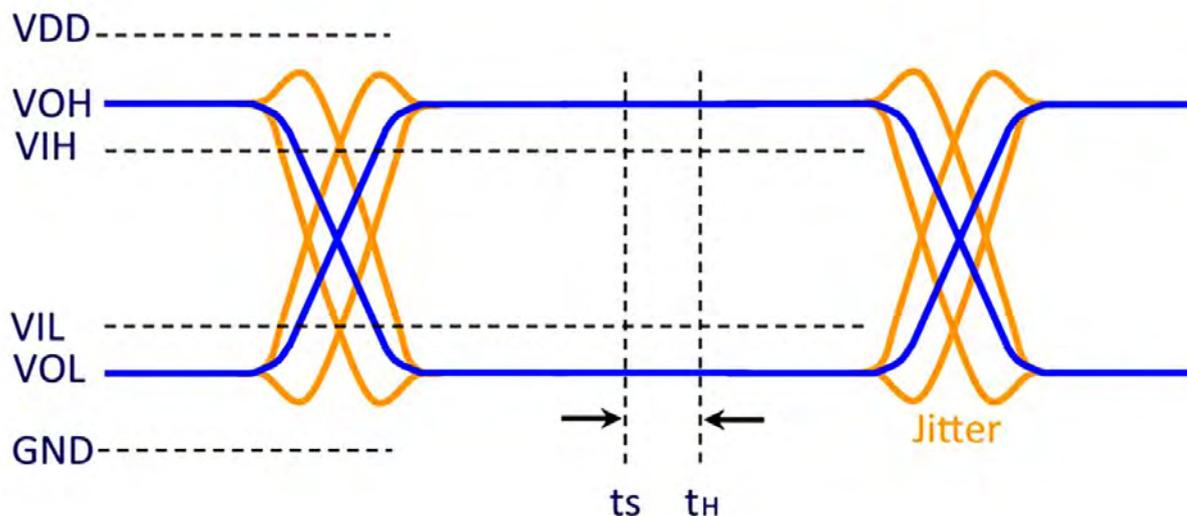


Figure 1: Crosstalk during the signal transitions only results in jitter of the eye.

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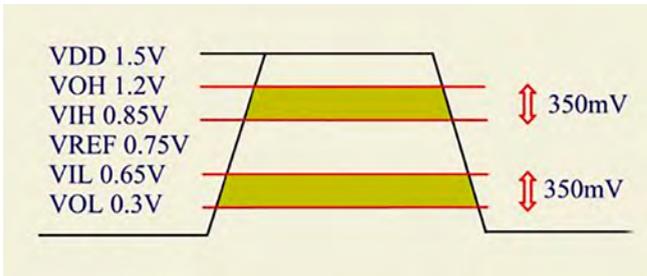


Figure 2: Noise margin for DDR3 memory.

on the eye. However, this only applies to signals within the same group. Asynchronous and unrelated signals, on the other hand, remain sensitive to crosstalk at all times.

Unfortunately, due to the ever-increasing speed of digital signals, one may not have the luxury of waiting so long to sample the bus. And as the supply voltage drops from say 3.3V to 1.5V, then the allowable noise margin more than halves making the circuit designer's decisions regarding crosstalk even more crucial. Crosstalk creates noise that erodes the noise margin. This noise may not be so great that it alone will cause a bit failure, but it can be enough to push the total noise over the edge.

For DDR3 memory devices for instance, the following values are taken from the JEDEC Specification JESD79-3E:

The maximum crosstalk value is the difference between the expected voltage at the receiver and the receiver threshold. In this case the maximum crosstalk is 350mV. This is for single-ended signals. Differential technologies do not have the noise margin concerns of single-ended technologies. This is due to common mode rejection, which is the ability of the receiver to reject noise that appears coincident on both inputs. Although differential technologies are much better at rejecting input noise, they are not totally immune. Excessive noise is still an issue and can cause serious problems.

Also, the crosstalk depends on the load which may vary considerably when driving banks of memory modules. Keep in mind that the total crosstalk on each victim trace is the total crosstalk from each of several nearby aggressors, all of which sum to produce the maximum value.

Figure 3 shows the near-end and far-end crosstalk for the victim traces adjacent to the aggressor trace (1.5V @ 1GHz). In this case

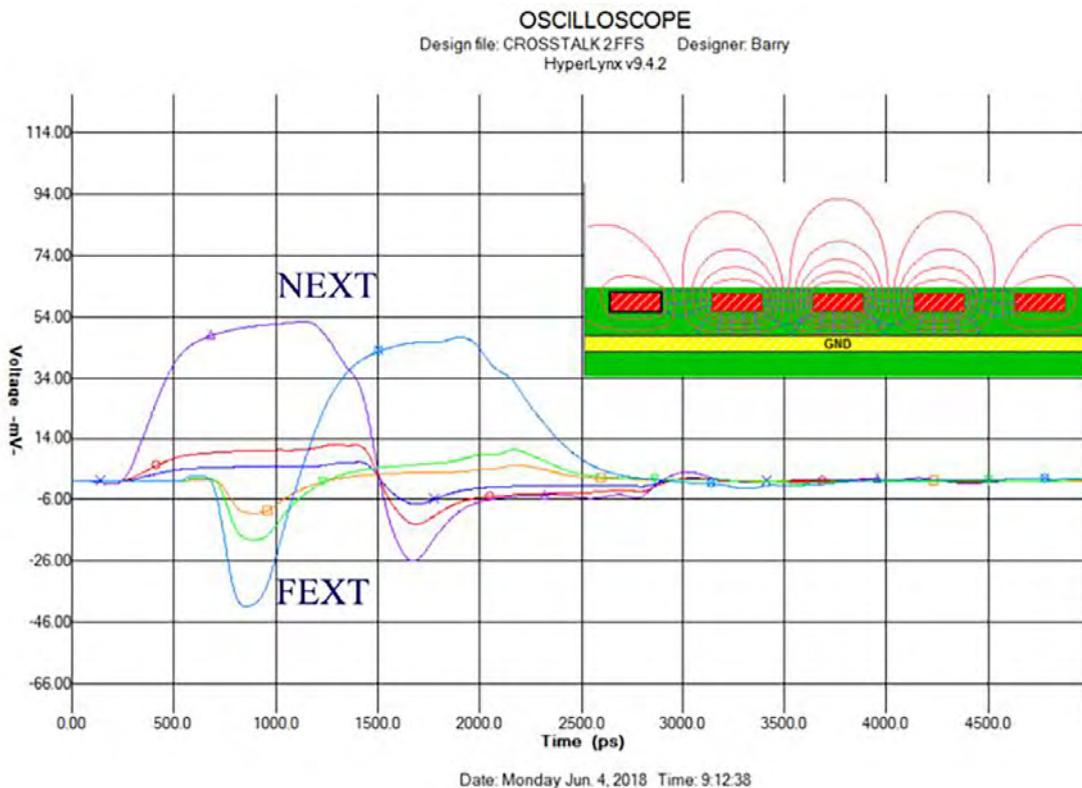


Figure 3: Near-end and far-end crosstalk for microstrip with 4/4 mil trace width/clearance.

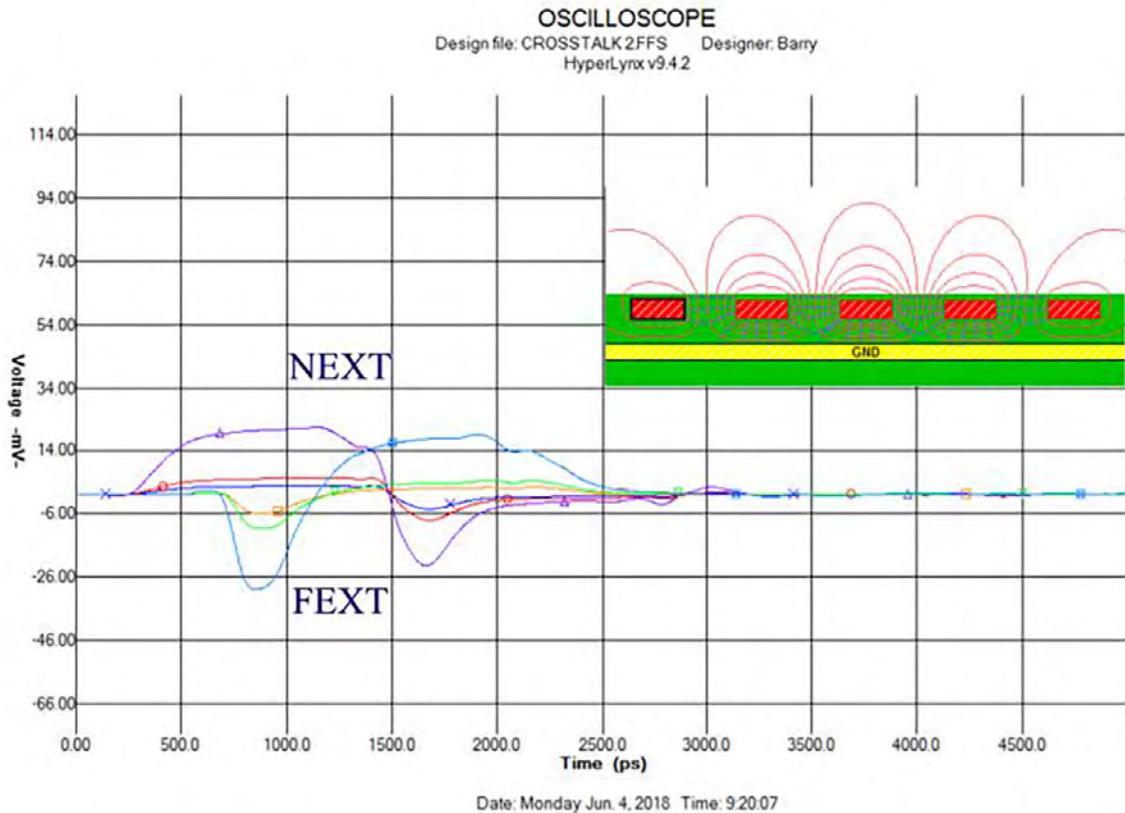


Figure 4: Near-end and far-end crosstalk for microstrip with 4/8 mil trace width/clearance.

the traces are 4 mil wide, 40 ohms impedance with a 4mil spacing. But, as the victim trace gets farther away from the aggressor the crosstalk decreases.

Figure 4 shows the near and far end crosstalk for 4 mil wide, 40 ohms impedance traces with 8 mil spacing. The further the separation the less the crosstalk. But, as previously mentioned, the total crosstalk on a victim trace is the accumulated noise injected from all nearby noise sources, so the result may be much more.

In a microstrip configuration, the mutual capacitive coupling, between adjacent traces, is generally weaker than the mutually inductive coupling, driving the FEXT co-efficient negative as can be seen in the previous simulations. However, forward crosstalk does not exist in the stripline configuration. The fine balance between inductive and capacitive coupled crosstalk produces almost no observable forward crosstalk.

Since the previous examples were of outer layer microstrip configurations, let's look at inner layer stripline crosstalk. Figure 5 shows

the near-end crosstalk of a stripline construction for 4 mil wide, 40 ohms impedance traces with a 4 mil spacing. Notice how there is no FEXT component of the noise. Also, the peak to peak amplitude of the crosstalk has been considerably reduced. So all other factors being equal, here is just another good reason why one should always route high-speed signals on the inner layers of a multilayer PCB.

One factor that may have been overlooked in this methodology is the effect on the signal of the transition from layer 1 to 3. At that point on the board, any power supply noise existing between the planes enters the memory bus circuit traces. This may be a major source of crosstalk, depending on the effectiveness of the power distribution network (PDN) decoupling. Excessive PDN noise at the jump location could completely swamp out the differences in crosstalk due to trace layout. This also presents another good reason why PDN analysis and optimization is so important.

To evaluate crosstalk, I typically run a preliminary batch mode simulation in Mentor

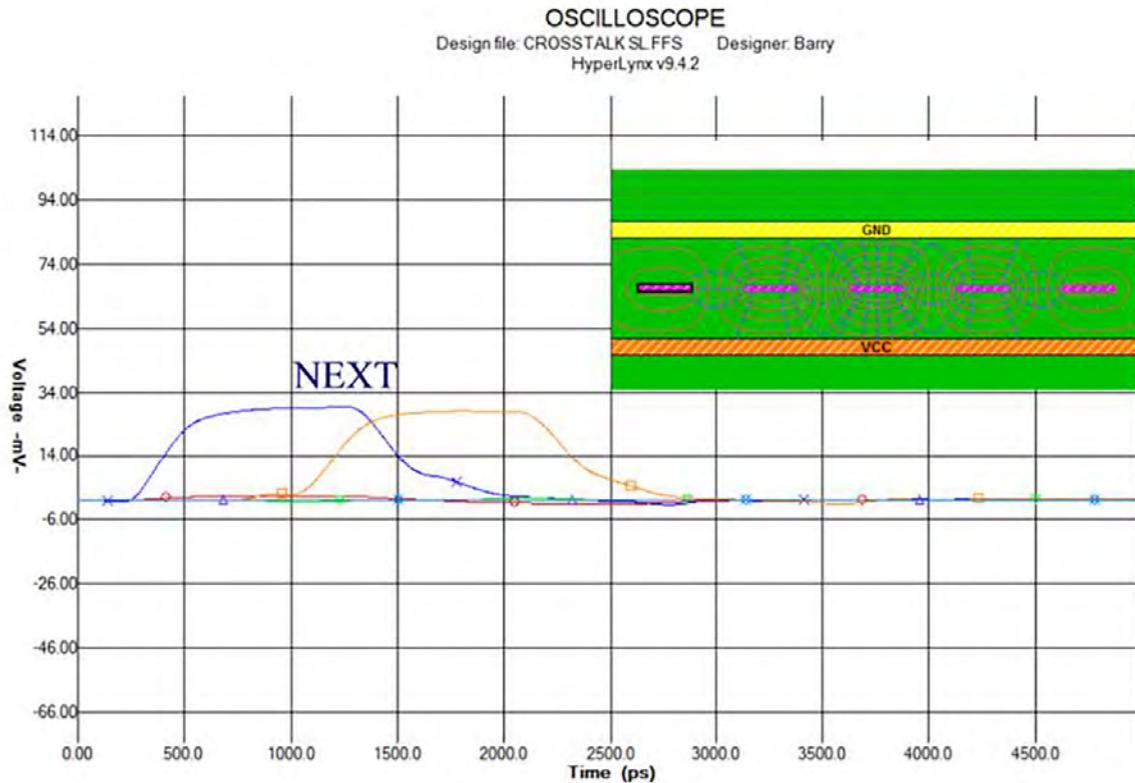


Figure 5: Crosstalk for stripline with 4/4 mil trace width/clearance.

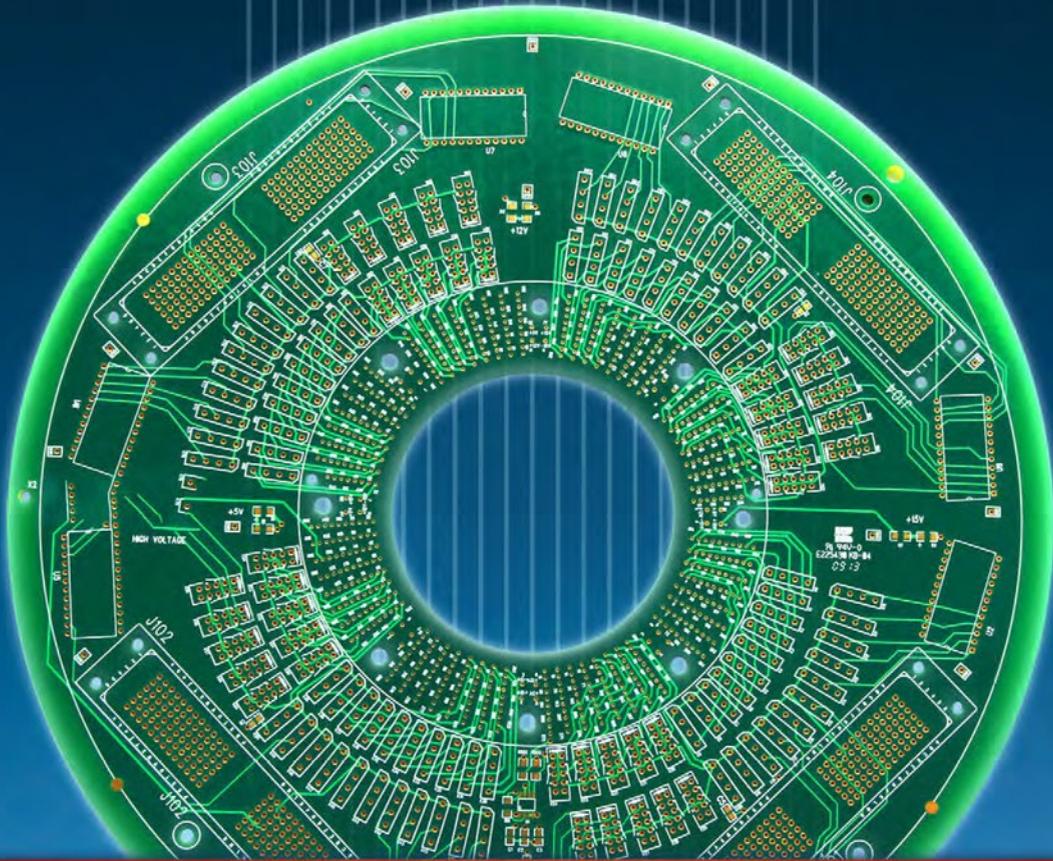
Graphics HyperLynx. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC Class B are setup in the simulator. The batch mode simulation automatically scans large numbers of nets on the entire PCB, flagging signal integrity, crosstalk and EMC hot spots. Reported crosstalk violations can be evaluated by further interactive simulation if required. Setting the simulator to 150mV maximum crosstalk, on all signals, may seem excessively low, considering the above, but it makes sure we pick up any coupling that may be detrimental to signal integrity when accumulated. I also apply this constraint to synchronous buses to identify the impact of the total crosstalk from all aggressors. It is much easier, and cost effective, to eliminate the source of the noise than to fix the problem further down the product development process.

Both forward and reverse crosstalk can be arbitrarily reduced by separating the aggressors from the victim traces or by reducing the height of the dielectric above/below the planes. The latter also requires a reduction in trace width

to maintain the impedance. Keep in mind that the fab costs generally increase below 4 mil trace width. So if real estate is a premium, as it generally is on dense, high-speed designs then reducing the dielectric height may be a good solution. We cannot completely eliminate crosstalk but as PCB designers, it is our job to ascertain how to control, manage and live with the consequences of our decisions.

Key Points:

- Reducing core voltage also reduces the noise margin.
- Crosstalk is caused by the coupling of the electromagnetic fields.
- Crosstalk falls off rapidly with the square of the distance and the degree of impact is related to the aggressor signal voltage and proximity.
- Synchronous buses benefit from an extraordinary immunity to crosstalk. It only has an impact within a small window around the moment of the clocking.



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- If the supply voltage drops from 3.3V to 1.5V, then the allowable noise margin more than halves.
- Differential technologies do not have the noise margin concerns of single-ended technologies. This is due to common-mode rejection.
- The total crosstalk on a victim trace is the accumulated noise injected from all nearby noise sources.
- Forward crosstalk does not exist in the stripline configuration. The amplitude of the crosstalk is also considerably reduced.
- The simulator should be set to 150mV maximum crosstalk on all signals. However, crosstalk from within the same group, on synchronous buses, can be ignored unless the frequency is extremely high.
- Both forward and reverse crosstalk can be reduced by separating the aggressors from the victim traces or by reducing the height of the dielectric above/below the planes.

References:

1. Barry Olney's Beyond Design columns: [Controlling the Beast](#), [A New Slant on Matched Length Routing](#), [Board-Level Simulation and the Design Process: Plan B – Post Layout Simulation](#).
2. [High-Speed Signal Propagation](#), by Howard Johnson.
3. All simulations performed in HyperLynx LineSim.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).

The Future of Electronics is Chemical

Molecular electronics, which aims to use molecules to build electronic devices, could be the answer. But until now, scientists haven't been able to make a stable device platform for these molecules to sit inside which could reliably connect with the molecules, exploit their ability to respond to a current, and be easily mass-produced.

An international team of researchers, including Macquarie University's Associate Professor Koushik Venkatesan, have developed a proof of concept device which

they say addresses all these issues. The team exploited the fact that metallic nanoparticles can provide reliable electrical contacts to individual molecules, allowing them to transport charge through a circuit.

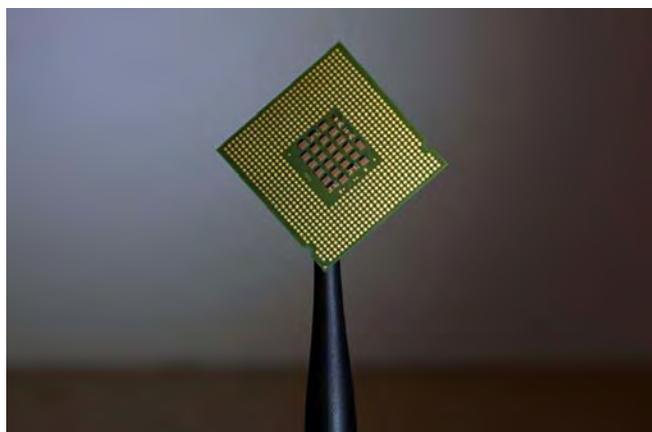
"Imagine a miniaturised transistor made up of several single molecules," says Koushik. "That's the promise of molecular electronics—devices that are smaller, faster, have more memory and are cheaper to make."

Koushik is confident their research will open up the bottleneck for this molecular-based technology to move forward.

"This fundamental research is extremely exciting as it points the way to practically 'wiring molecules' by exploiting the fact that Koushik and his colleagues have made a metallic nanoparticle provide a reliable electrical contact to individual molecules," says Professor Alison Rodger, Head of the Department of Molecular Sciences at Macquarie University.

"It is amazing to think that this work leads the way to true molecular-sized electronic circuits."

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Are Solvent-Free, Water-Based Coatings Reliable?

Sensible Design

by Phil Kinner, ELECTROLUBE

At a time when we should all be considering the impact that some conformal coating formulations can have on the environment and start looking for more environmentally friendly options, let me pose this question: How effective can water-based conformal coatings really be?

In my first column in this series, I looked at how to minimise and limit incidences that may hinder the performance of conformal coatings. Essentially, I offered advice on the most appropriate product selection, application technique and the key decisions on a range of issues, such as how thick the coating should be.

However, one area I didn't cover in my last column is how the various chemistries that underpin these high-performing products affect the environment—either during application (when they may potentially pose a hazard to workers) or in the context of their role as pro-

tection for electronic assemblies that are put to use in the wider world. In this column, I intend to concentrate fully on environmental factors, describing the environmentally friendly products that are in operation and upcoming, and their limitations.

With environmental awareness at an all-time high, companies are looking for greener options in terms of the chemical products they use for the manufacture and protection of electronics, including conformal coatings and various cleaning technologies, among others. Such products often contain solvents, which are described as volatile organic compounds (VOCs), carbon containing substances that vaporise easily at room temperature.

From a raw materials perspective, and concentrating on chemicals used within the electronics sector, there is now a greater choice of more environmentally friendly alternatives



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available for design engineers to consider. In recent years, such alternatives have progressed considerably in terms of their performance as protectors of electronic circuits while complying with increasingly onerous environmental constraints and internationally recognised standards.

Water-based coatings are a case in point. For instance, all of us have now become used to using water-based paint products that have very little odour when applied and thankfully make brush cleaning much easier and less messy. Indeed, water-based paints now dominate the market for internal decorative applications. We also have had water-based conformal coatings for more than a decade, but in an electronics context, and particularly where they are used as a corrosion prevention medium, they have two major limitations.

The first one is obvious: They contain water. Water is electrically conductive and water-based coatings can remain sufficiently conductive for many, many months after application, creating signal integrity or crosstalk issues on sensitive board designs. Secondly, to prepare the emulsions or dispersions, some form of compatibility with water is necessary, being either a modification of the polymer (dispersion) or surfactant (emulsion). The problem with either approach is that both types remain somewhat sensitive to water throughout their lifetimes, thus limiting the protection they can afford in high humidity environments.

Overall, the performance of current water-based materials is not comparable with that of solvent-based resins and is very far from the performance of solvent-less materials. However, with the current levels of R&D activity being conducted into the development of viable water-based systems, I am confident that these limitations will eventually be overcome.

Key Benefits of Solvent-Free

Solvent-free materials are generally lower-odour, lower-hazard materials and are therefore much safer for users to apply at the manufacturing stage. They are usually non-flammable and consequently pose a lower insurance risk both at the production stage as well as in

use. Significantly, they help minimise levels of VOC emissions, ensuring compliance with environmental standards. Where 2K (two-part) conformal coatings are concerned, it is possible to apply thicker coatings and achieve better protection without compromising other performance requirements such as tolerance of thermal shock.

Clearly, some coatings must be able to perform in exceptionally harsh environments, so what might be a typical combination of elements that represents the harshest environment that a coating must protect against? Let's take corrosion as an example; for a metal surface to corrode, a potential difference, electrolyte and ionic impurities must all be present. If a coating is well applied, it will prevent corrosion by inhibiting external ionic species and liquids such as water from reaching the metal surface.

Let's take corrosion as an example; for a metal surface to corrode, a potential difference, electrolyte and ionic impurities must all be present.

Any environment that can cause degradation of the coating and provide the required conditions for corrosion to occur can potentially be tough on the coating. For example, an environment in which there is cycling between high and low temperatures places the coating under a lot of stress, while an abnormally high temperature can speed up polymer degradation; these conditions can combine to cause cracking of the coating, exposing parts of the circuit to impurities which will ultimately lead to circuit failure. The cyclical nature of the thermal environment will create differences between the board and its local ambient conditions, leading to the formation of damaging condensation. Should the assembly also be exposed

to salt-spray then the likelihood of failure will increase significantly.

Test, Test and Test Again

Environmental testing methods are the key to ensuring that coatings are fit for purpose and will stand up to the most rigorous of conditions. But what exactly is environmental testing? In its basic form, environmental testing is conducted on a material to ascertain its performance characteristics under controlled environmental conditions as close as possible to those in which the product may reasonably be expected to perform.

Examples include, but are not limited to, the following: extremely high and low temperatures; rapid excursions of temperature sufficient to impose thermal shock; salt spray and salt fog; very high humidity or condensing conditions; saturated environments; exposure to fungal growths, corrosive gases and solar radiation, and high and low atmospheric pressures (especially for aeronautical and space equipment).

In addition to understanding how well the material tolerates each individual condition, these specific tests form the basis for sequential testing by a combination of methods to evaluate the cumulative effects of harsh environments. A coated board will be subjected to a variety of environmental impacts, not just one. The conditions and exposures should be chosen to be representative of what could reasonably be expected in a real life, end-use environment.

So, there you have it. Environmentally friendly materials are available now and new developments are coming online. As their performance gradually improves, with time these materials will open new avenues for compliance across many disciplines.

A cautionary note for the present, however: Test your water-based conformal coating thoroughly and ensure that it meets your immediate needs while delivering a guaranteed level of protection.

DESIGN007



Phil Kinner is the global business/technical director of the coatings division of Electrolube. He is also the author of *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*.

A Step Closer to Single-Atom Data Storage

In a new study published in *Physical Review Letters*, physicists at EPFL's Institute of Physics have used Scanning Tunneling Microscopy to demonstrate the stability of a magnet consisting of a single atom of holmium, an element they have been working with for years.

"Single-atom magnets offer an interesting perspective because quantum mechanics may offer shortcuts across their stability barriers that we could exploit in the future," says EPFL's Fabian Natterer who is the paper's first author. "This would be the last piece of the puzzle to atomic data recording."

Using a scanning tunneling microscope, which can "see" atoms on surfaces, the scientists found that the holmium atoms could retain their magnetization in a magnetic field exceeding 8 Tesla, which is around the strength of magnets used in the Large Hadron Collider. The authors describe this as "record-breaking coercivity," a term that describes the ability of a magnet to withstand an external magnetic field without becoming demagnetized.

"Research in the miniaturization of magnetic bits has focused heavily on magnetic bistability," says Natterer. "We have demonstrated that the smallest bits can indeed be extremely stable, but next we need to learn how to write information to those bits more effectively to overcome the magnetic 'trilemma' of magnetic recording: stability, writability, and signal-to-noise ratio." [Click here for more.](#)





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The U.S. defense industrial base—and the electronics industry in particular—would benefit from a provision in a newly released U.S. Senate bill. IPC welcomes the U.S. Senate's version of the National Defense Authorization Act (NDAA).

Catching up with Fineline-Global N. American CEO Eran Navick ▶

After entering the North American marketplace just six months ago, printed circuit board provider Fineline-Global is making its mark. A value-added PCB supplier, Fineline prides itself on being any able to meet any challenge for any company in any part of the world.

Nano Dimension Now Certified U.S. DoD Vendor ▶

As a registered and approved vendor, Nano Dimension is now positioned to pursue and conduct business directly with the U.S. federal government and its many agencies, including the Department of Homeland Security and other United States Department of Defense entities.

Sanmina's Costa Mesa Facility Achieves AS9100D Certification ▶

Sanmina Corporation announced that its technology center in Costa Mesa, California, has earned AS9100D certification for defense and aerospace manufacturing.

President Trump Announces 25% Tariff Imposition on Chinese Imports ▶

President Trump announced that he will impose 25% tariffs on Chinese imports worth roughly \$50 billion. The tariffs are the result of an investigation that found China's technology transfer policies had harmed U.S. companies.

NASA Technology Managers Visit TopLine at Space Tech Expo ▶

Members of the NASA Technology Licensing and Commercialization Team visited the TopLine exhibit at the recent 2018 Space Tech Expo show, where they awarded a NASA lapel pin to TopLine CEO Martin Hart.

FTG Inks Long-Term Agreements with Rockwell Collins ▶

The award incorporates a variety of technologies for use on major airframe platforms across business, regional, air transport and government systems market applications and consists of multi-year awards up to five years.

US Defense Military Satellite Sector Fueled by Heightened Funding against Escalating Cyber Warfare ▶

Modernization strategies along with counter and offensive space initiatives create significant growth opportunities that could take the market past \$30 billion by 2023, finds Frost & Sullivan.

Design and Manufacturing Perspectives from DISH Technology's Les Beller ▶

Interview with Les Beller, a long-time PCB designer who is now a manufacturing engineer for DISH Technology. We discussed his company's business shift towards 5G and streaming, and the stresses that puts on a design team.



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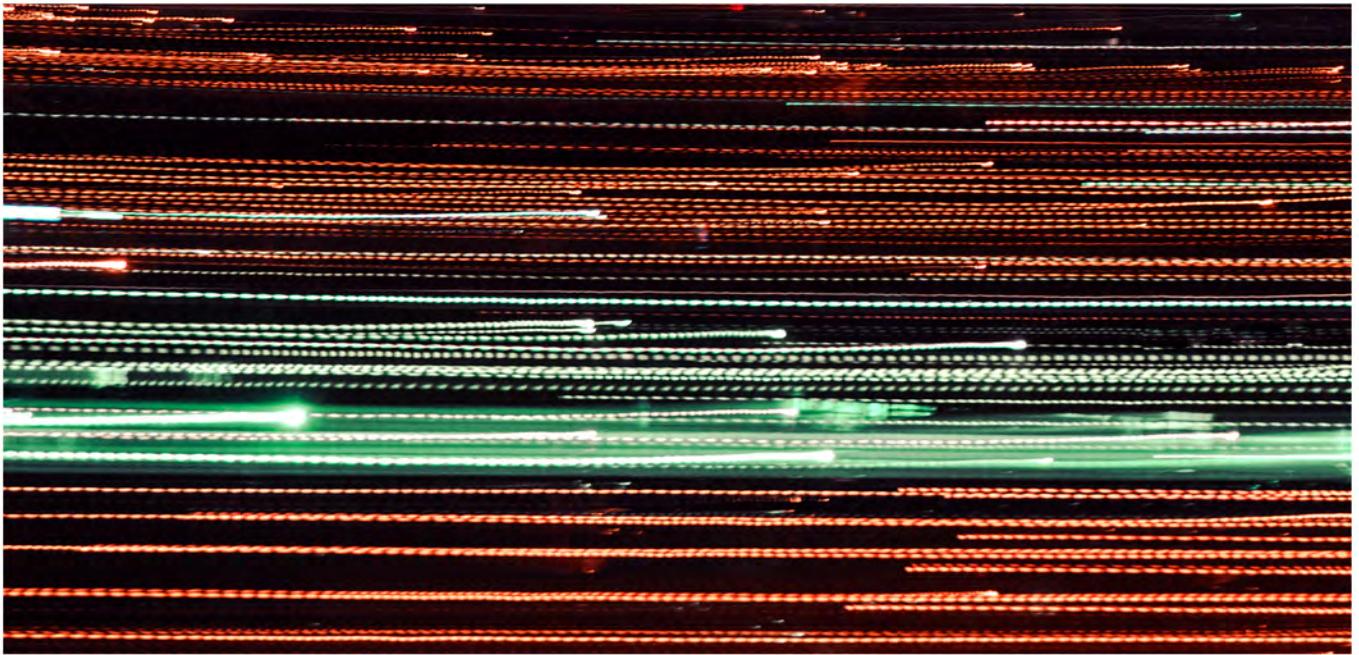
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Advanced Stackup Planning with Impedance, Delay and Loss Validation

Article by Yuriy Shlepnev
SIMBERIAN INC.

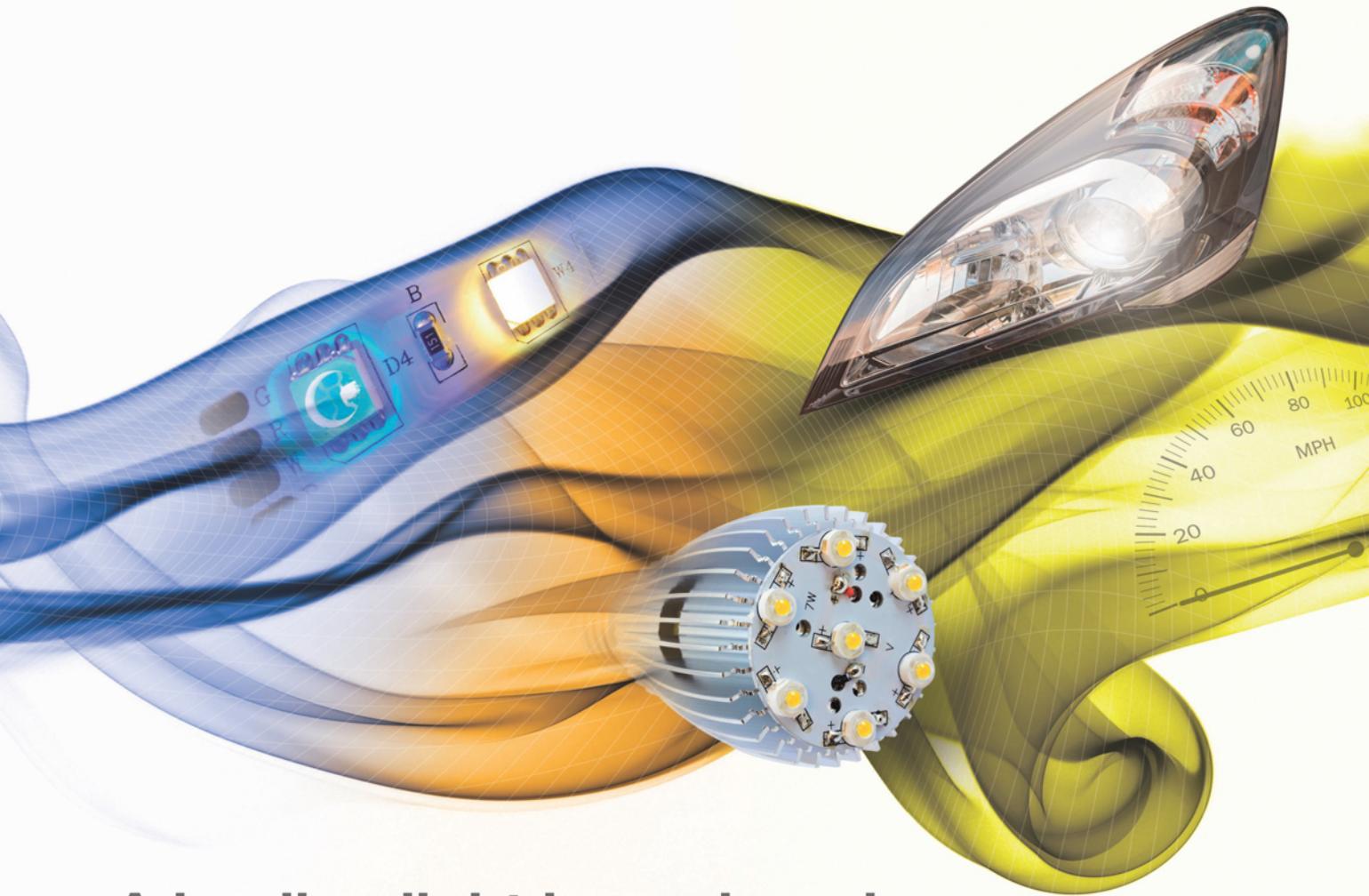
A typical PCB design usually starts with the material selection and stackup definition—the stackup planning or design exploration stage. How reliable are the data provided by the material vendors and PCB manufacturers? Can we use these data to predict trace width and spacing for the target trace impedance or to calculate delays or evaluate the loss budget?

PCB routing is usually done with these preliminary data. The actual stackup may be further adjusted by the PCB manufacturer together with the trace widths and spacing, to have the target impedances. This is the typical impedance-controlled process that is well established and usually produces an acceptable outcome.

But what about the losses? Can we use preliminary data to evaluate the losses and loss-related compliance metrics? Or can we just specify the target losses and rely on the manufacturers, as is done with the impedance? Let's try to answer these questions. An EvR-1 vali-

ation board is used here as an example with the preliminary and final data—all data for this board are provided by Marko Marin from Infinera. This board was featured in our award-winning “Expectation vs. Reality” paper ^[1]. We will use Simbeor software as the stackup exploration tool to evaluate the accuracy of the characteristic impedance, delay and losses. Simbeor is selected for the stackup exploration because it is systematically validated with the measurements up to 50 GHz ^[2].

Stackup planning begins with selecting a PCB manufacturer and possible materials and defining the stackup structure. In our case, the validation board has 20 layers with 8 layers assigned for the high-speed signals as shown in Figure 1. Low-loss Panasonic Megtron6 laminate is selected to rout the high-speed interconnects. The target impedance has been specified for the PCB manufacturer, and the manufacturer has provided expected stackup structure, trace widths, and spacing adjustments to fulfil the target impedances ^[1]. This is the usual case for a production board.



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According to the manufacturer, the expected impedance variations should be within 8%. That is too large to expect excellent correlation up to 30 GHz for 28 Gbps NRZ links, but it may be acceptable. The board manufacturer provided stackup geometry as shown in Figure 1 on the left side, and corresponding stackup entered for the pre-layout analysis into Simbeor software is shown on the right side. Megtron6 specs provide dielectric constant and loss tangent at multiple frequencies—just one frequency data can be used to define causal wideband Debye model. The values for Dk in the Figure 1 are slightly different from the Megtron6 specs and are provided by the PCB manufacturer based upon their experience with this material.

The major problem here is with the conductor roughness models—all we know that the copper foil roughness is specified as H-VLP and no other data. PCB manufacturer also roughens the shiny side of the copper foil during the board manufacturing, without any parameters for the electrical modeling. Even if we had data for the mate side of the copper foil from the copper foil manufacturer, the PCB manufacturer treatment of the shiny side makes it practically useless. Thus, we start the stackup exploration without the conductor roughness model and with the trace adjustments provided

by the PCB manufacturer. The rest of the EvR-1 validation board design is covered in detail in this paper [1]. To validate the preliminary data, we will use 10 cm differential links in strip layer INNER1 and microstrip layer BOTTOM (Figure 1). The results of the first experiment are shown in Figure 2. Left graphs show measured TDRs—the response is computed with S-parameters measured up to 50 GHz. TDRs for 10 cm segments of the transmission line model computed in Simbeor are also shown on the same graphs for comparison.

We can see acceptable TDR correlation for the strip line, but computed impedance of the microstrip line is substantially lower. The models for these preliminary comparisons do not have the launches. Right graphs in Figure 2 show correlation between the generalized modal S-parameters (GMS-parameters) measured and computed for 5 cm segment of the differential lines. GMS-parameters are reflectionless transmission parameters; the reflection losses are completely removed in Simbeor software. That makes this type of S-parameters ideal for precise material parameters identification and model quality evaluation. From GMS-parameters we can observe that the model delays are off by less than 2 ps/inch. The most important is the obvious difference in the losses—the difference

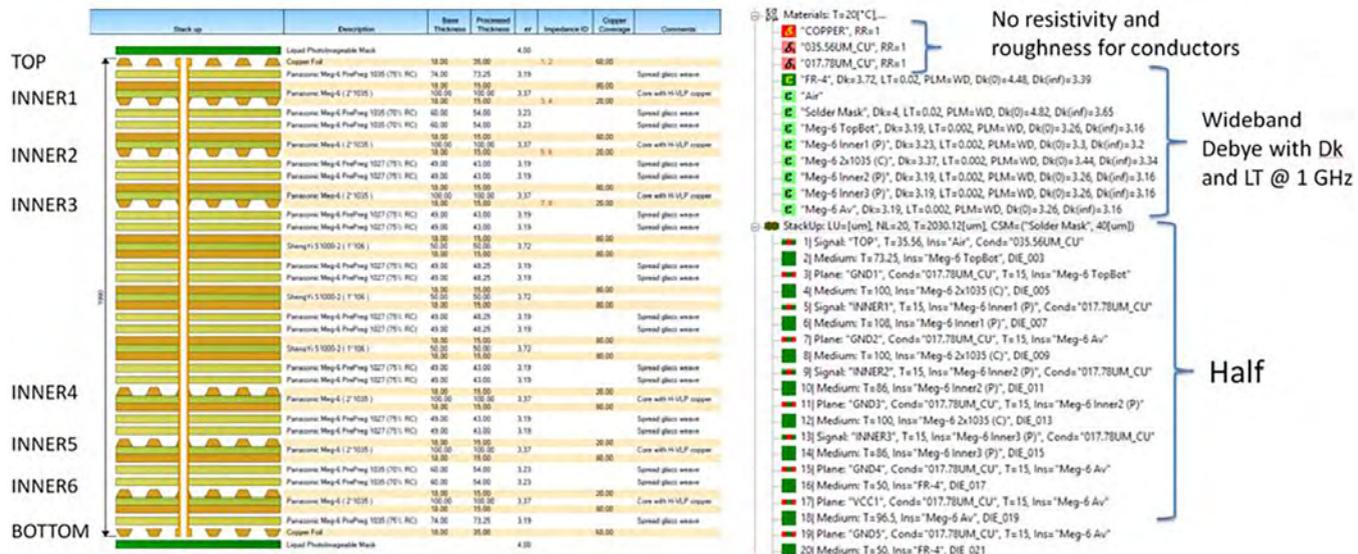


Figure 1: The EvR-1 validation board stackup from the PCB manufacturer (left) and the initial material models, and exactly the same stackup in Simbeor software defined for pre-manufacturing analysis (right).

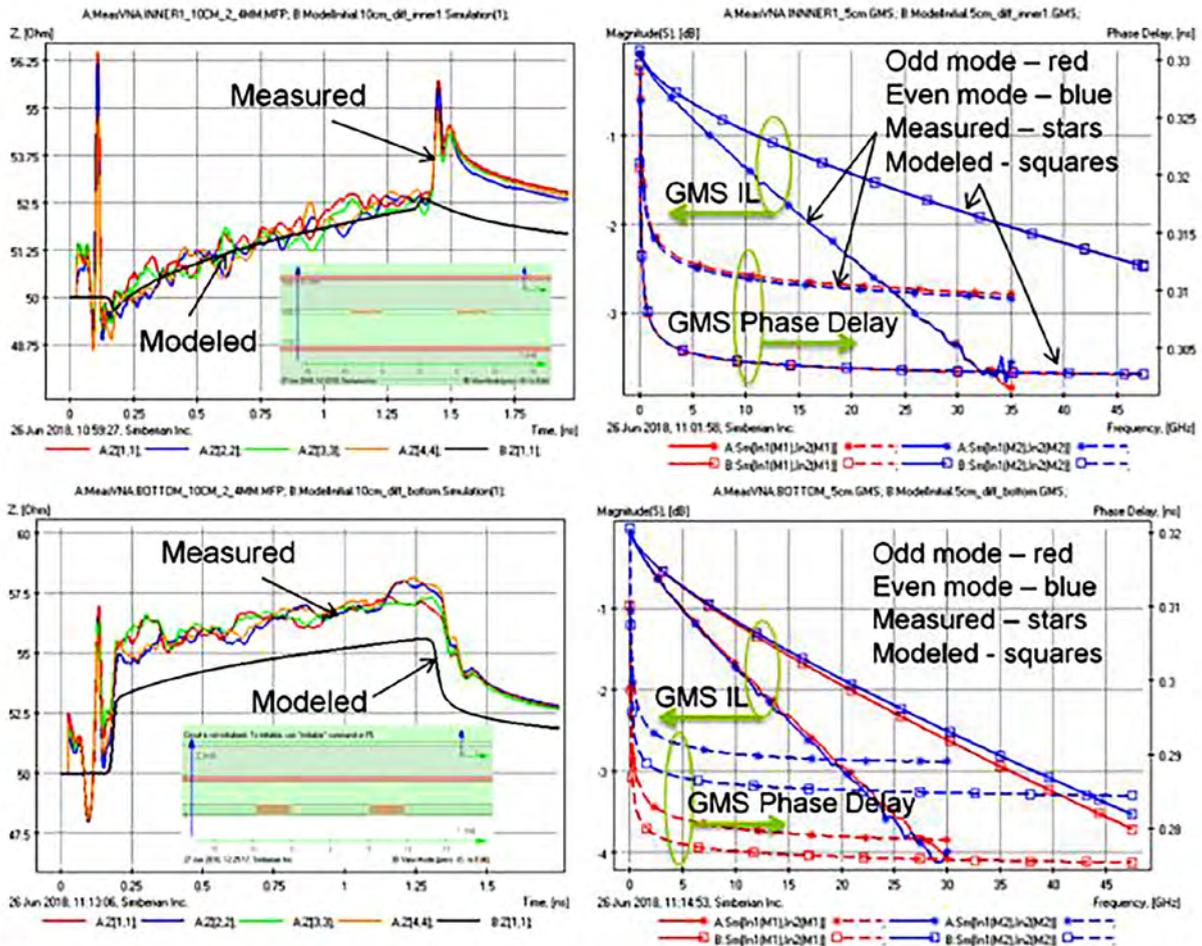


Figure 2: TDR of 10 cm differential links measured and computed (left graphs) and GMS insertion loss (IL) and phase delay for 5 cm differential line segments measured and computed (right graphs) with the stackup structure and material parameters from the PCB manufacturer for layer INNER 1 (top graphs) and for layer BOTTOM (bottom graphs).

is already substantial at 5 GHz (about 20%) and may be totally un-acceptable at 30 GHz (about 50%).

So, why do we see such discrepancies between the measurements and models? For the losses, it is quite obvious: We do not have any data at the stackup exploration stage to specify conductor roughness models. If such models are used to compute compliance metrics, it can lead to complete design failure!

Note that this is not just a problem related to losses; it also affects such metrics as the insertion loss to power sum crosstalk metric (ICR). Considering differences in the impedances and delays, it is either differences in the geometry of the cross-sections or in the parameters of the dielectrics or both. We will find out soon.

To make it more complicated, note that the conductor roughness increases the inductance of the traces and can substantially change both the impedance and phase delay in addition to the losses [3]. All that must be included in the transmission line model. Also, simple adjustment of the model parameters (geometry or dielectric properties) will not work; too many parameters to play with and a systematic approach is needed. Fortunately, with Simbeor software the parameters of the dielectric and conductor roughness models can be separately identified in the systematic way.

It can be done with the S-parameters measured for two-line segments and converted into either GMS-parameters, or into complex propagation constants (Gamma). Both GMS-

parameters and Gamma can be used in Simbeor to identify the material properties with the separation of the losses between the dielectric and conductor roughness [4]. For the accurate and unique identification, the geometry of the transmission lines in the test structures must be measured from the cross-sections. The EvR-1 board was cross-sectioned and investigated. The final trace widths and separations with an example of the cross-sections are shown in Figure 3.

What we can learn from this is that the trace widths and space adjustments from this particular PCB manufacturer were acceptable only for the striplines. However, the geometry of the microstrip traces in the BOTTOM or TOP layers are completely different from the data provided by the manufacturer. That is why we observe more differences in TDR of the microstrips in Figure 2. See more observations and the material identification step details and references in [1].

The final stackup with all geometry adjustments from the microphotographs and dielectric and conductor roughness models identified with Simbeor software is shown in Figure 4. To ensure the accuracy, we have 8 dielectric models - one for the core dielectric, four for the prepreg layers, one for solder mask dielectric and two optional for the resin-rich layers surrounding

the strips in the interior layers. The resin-rich layers are required only in cases when test structures have some far end crosstalk (FEXT) and it has to be accounted for in the model. Dielectric constants and loss tangents from the PCB manufacturer are shown in brackets in Figure 4 for comparison. In addition to the dielectrics, two conductor roughness models are identified—there is nothing to compare it with. The analysis to measurement correlation with all that adjustments and material models are shown in Figure 5. Comparing to the results with the data from PCB manufacturer shown in Figure 2, the correlation is much better. Though, it is not perfect due to the expected manufacturing variation and possibly other unknown reasons that we may further discover. With this new stackup, both pre- and post-layout analysis can be done with high confidence as demonstrated in [1] and [2].

The bottom line is that the stackup data provided by a PCB manufacturer must be validated. Data for strip line layers from this particular manufacturer were basically acceptable for the preliminary analysis of the impedances and delays in the strip lines. Though, data for the traces in the surface layers (microstrips) were not acceptable to do any analysis. Most troubling was the absence of models or any useful data to build conductor roughness mod-

Designed trace dimensions:	Dimensions from manufacturer:	Dimensions after cross-sectioning:
BOTTOM: 120-250-120 [um]	BOTTOM: 112-258-112 [um]	BOTTOM: HAT(89/97)-260-HAT(89/97) [um]
INNER1/6: 110-250-110 [um]	INNER1/6: 107-250-107 [um]	INNER1/6: 107-255-107 [um]
INNER2/3: 100-250-100 [um]	INNER2/3: 99-245-99 [um]	INNER2/3: 96-254-96 [um]
INNER6 SE: 110 [um]	INNER6 SE: 109 [um]	INNER6 SE: 109 [um]
BEATTY INNER1 and INNER6:		BEATTY INNER 6:
110 um 2.5 cm, 330 um 2.5 cm		109 um 2.5 cm + 326 um 2.5 cm

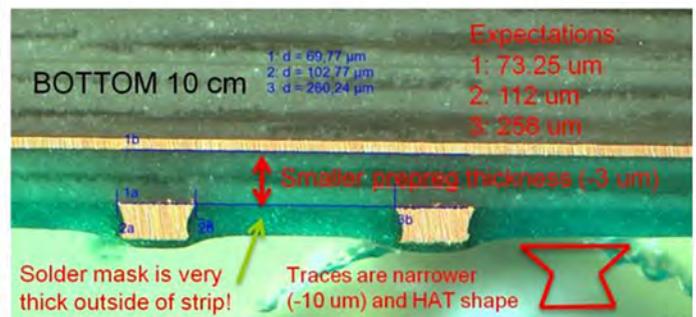
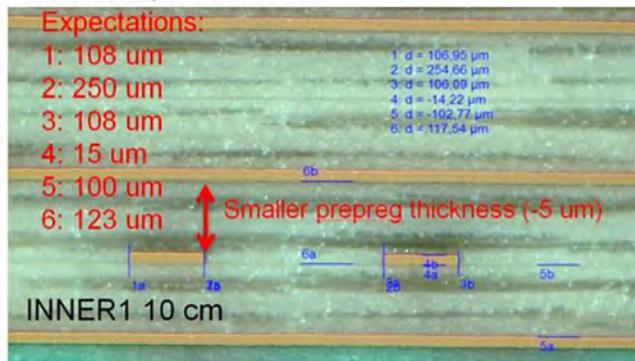


Figure 3: Final trace geometry adjustments and example of the cross-sections of differential test links in INNER1 and BOTTOM layers (expectations are data from PCB manufacturer).

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Huray-Bracken Roughness Models (causal):
 Strips: SR=0.098 um, RF=12.5
 Microstrips: SR=0.229 um, RF=3.77

Wideband Debye models, Dk and LT @ 1 GHz (initial in brackets):
 CORE (all layers): Dk=3.37 (3.37), LT=0.003 (0.002)
 Prep. INNER1/INNER6: Dk=3.17 (3.23), LT=0.003 (0.002)
 Resin INNER1/INNER6: Dk=3.562, LT=0.003
 Prep. INNER2: Dk=3.124 (3.19), LT=0.002 (0.002)
 Resin INNER2/INNER3: Dk=3.09 (3.19), LT=0.002 (0.002)
 Resin INNER3: Dk=3.425, LT=0.002 (0.002)
 TOP/BOTTOM: Dk=3.4 (3.19), LT=0.006 (0.002)
 Solder Mask: Dk=3.2 (4.0), LT=0.02

2 roughness models and 8 dielectric models – more difficult to identify, but is necessary for FEXT analysis

Figure 4: The final stackup structure and dielectric and conductor roughness models.

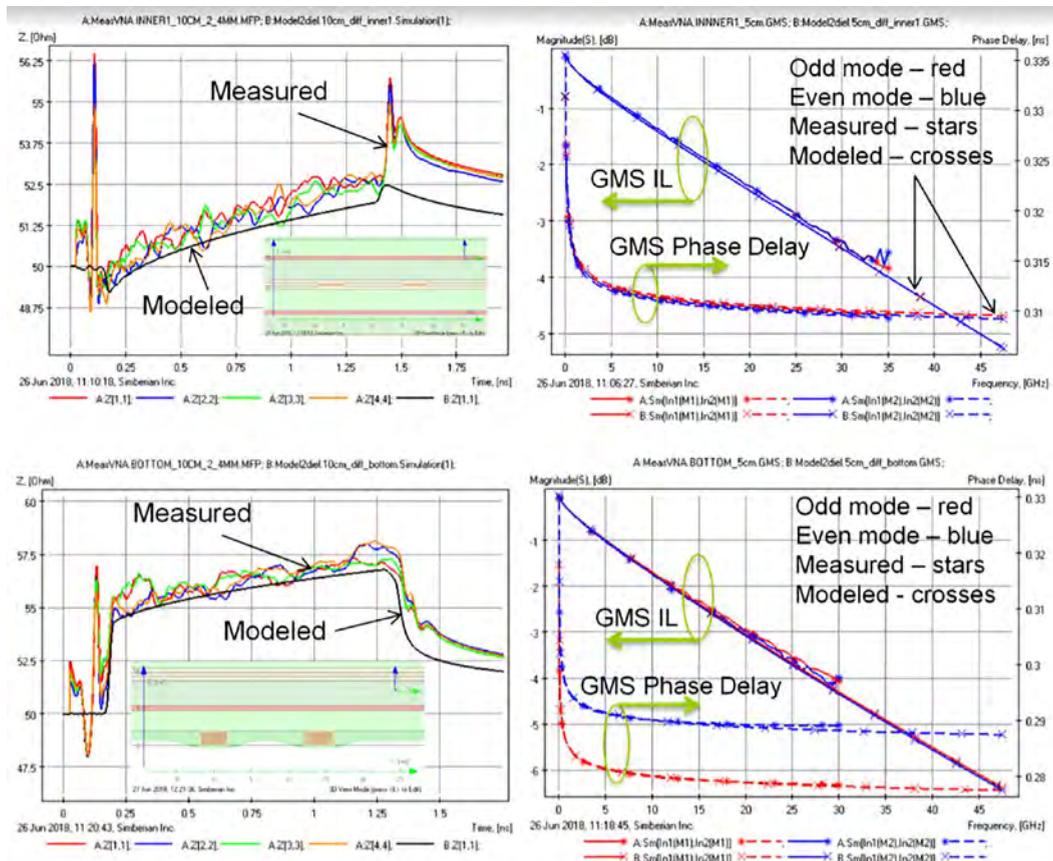


Figure 5: TDR of 10 cm differential links measured and computed (left graphs) and GMS insertion loss (IL) and phase delay for 5 cm differential line segments measured and computed (right graphs) with the identified stackup structure and material models for layer INNER 1 (top graphs) and for layer BOTTOM (bottom graphs).

els; any investigation of the losses would be completely useless without such models. Thus, any stackup exploration or planning stage must include building small validation boards or test coupons to verify the data obtained from the PCB manufacturer and to identify actual geometry adjustments and the conductor roughness models. The coupons should have two segments of transmission line (single-ended or differential) with different lengths per each layer with unique dielectric. The coupons must be cross-sectioned after S-parameters of the line segments are measured. This is the most important step of the systematic approach to design predictable interconnects. **DESIGN007**

Simbeor software was used for all computations provided in this article. All corresponding Simbeor solutions are available upon request to learn the “sink or swim” process.

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award-winning paper from DesignCon2018, January 31, 2018, Santa Clara, California. Presentation with complete report [is also available here](#).

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Yuriy Shlepnev is founder and president of Simberian Inc.

NASA, Partners, Advance In-Space Assembly Robotics

The first week of July 2018 marked the last in a series of ground tests demonstrating the capabilities of the Tendon Actuated Lightweight In-Space MANipulator (TALISMAN) robotic arm; the Strut Assembly, Manufacturing, Utility & Robotic Aid (SAMURAI); and the NASA Intelligent Jigging and Assembly Robot (NINJAR) components of the Commercial Infrastructure for Robotic Assembly and Services (CIRAS) project.



Earlier this year, the team of engineers manipulated the newer, longer arm back and forth from folded to extended positions to demonstrate that it is fully operational, then they showed it could pull a truss out from being stowed in a compartment. In this demonstration, the TALISMAN arm was used to move a solar array from one truss section to another and to install the array.

SAMURAI, the robotic hand that passes truss parts, and NINJAR, the jigging robot that holds the pieces in place while they are fastened, have similarly been put to the test this year. The team first used a remote control to operate the two robots and assemble truss segments. This most recent test accomplished an autonomous truss build, using only code and no remote control.

CIRAS is a part of the In-Space Robotic Manufacturing and Assembly (IRMA) project portfolio, managed by NASA's Technology Demonstration Missions Program and sponsored by NASA's Space Technology Mission Directorate. [Click here for more](#).



Recent Highlights from Design007

1 Altium Sponsors Seven Teams at 2018 SpaceX Hyperloop Pod Competition ▶

Altium will sponsor seven teams at SpaceX's upcoming 2018 Hyperloop Pod Competition, which will take place on Sunday, July 22, 2018 at SpaceX's headquarters in Hawthorne, California.

2 Faster Board Speeds Demand Constraint-Driven Design ▶

Constraints become increasingly important as components and boards become faster and more complex. But it is hard to capture and use/obey these constraints consistently throughout the complete design process, bearing in mind that may contradict each other. The Post-it Note captures this idea particularly well. A brief sketch implicitly includes the constraints that the designer is working under, in a very concise form; however, retaining and using this information later is extremely difficult.



3 Proteus Users Can Access EMA's Ultra Librarian 14 Million-Part Database ▶

The Proteus Design Suite is a complete EDA software solution for professional PCB design, comprising schematic capture, microcontroller simulation, and PCB layout. With this latest update to Ultra Librarian, Proteus users will be able to export symbols and footprints in the Proteus format from UltraLibrarian.com or the Ultra Librarian desktop software.

4 Paving the Way for 400Gb Ethernet and 5G ▶

This article briefly introduces the 4-level pulse amplitude modulation (PAM-4) and its application in 400 Gigabit Ethernet (400GbE), to support the booming data traffic volume in conjunction with the deployment of 5G mobile communications.



5 Dave Wiens Discusses Multi-board Design Techniques ▶

For our multi-board design issue, I interviewed Dave Wiens, product marketing manager for Mentor, a Siemens business. We discussed how the multi-board design technique differs from laying out single boards, along with the planning, simulation and analysis processes required to design multi-board systems.



6 CUI Partners with SnapEDA to Offer Free PCB Footprint Files ▶

“We are committed to building the industry’s largest, verified library of component models. Adding CUI and their broad portfolio of board level components to our catalog supplies yet another source from which engineers can gather PCB files for seamless integration into their designs,” said Natasha Baker, CEO of SnapEDA.



7 Making the Most of PCB Materials for 5G Microwave and mmWave Amps ▶

5G represents the latest and greatest in wireless technology, and it will be challenging to design and fabricate, starting with the circuit board materials, because it will operate across many different frequencies, such as 6 GHz and below, as well as at millimeter-wave frequencies (typically 30 GHz and above). It will also combine network access from terrestrial base stations and orbiting satellites.



8 Beyond Design: Common Symptoms of Common-Mode Radiation ▶

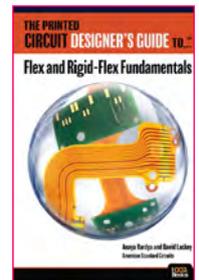
Unfortunately, differential-mode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by signal skew, rise/fall time mismatch or asymmetry in the channel. Also, return path discontinuities can create large common mode loop areas that increase series inductance and electromagnetic radiation. In this month’s column, I will explore the common symptoms of, and present some cures for, common mode radiation.

9 iCD Introduces the New Materials Planner Software ▶

In-Circuit Design Pty Ltd (iCD), Australia, developer of the iCD Design Integrity software, has released the new iCD Materials Planner software to add to the Stackup Planner functionality. This will be rolled out to iCD support customers as an update to their current software.

10 Excerpt: The Printed Circuit Designer’s Guide to...Flex and Rigid-Flex Fundamentals ▶

The design process is arguably the most important part of the flex circuit procurement process. The decisions made in the design process will have a lasting impact, for better or worse, throughout the manufacturing cycle. In advance of providing important details about the actual construction of the flex circuit, it is of value to provide some sort of understanding of the expected use environment for the finished product.



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